SpectralBER System

10G Installation and System Reference Manual (Part No. J1420-90017)

Where to Find it - Online and Printed Information:

System installation (hardware/software) ..	VXIbus Configuration Guide* This Manual
Module configuration/control	This Manual J1420B Receiver DWDM Receiver and J1421A/J1422B/J1426A/J1427A Clock Source/MTS/BITS and Transmitter Module User's Manual
SCPI information	SpectralBER System 10G Remote Control Manual
VXI programming	SpectralBER UID Online Help
VXI example programs	SpectralBER UID Online Help SpectralBER System 10G Remote Control Manual This Manual
VXI function reference	SpectralBER UID Online Help
Soft Front Panel information	This Manual J1420B Receiver DWDM Receiver and J1421A/J1422B/J1426A/J1427A Clock Source/MTS/BITS and Transmitter Module User's Manual SpectralBER UID Online Help
VISA language information	VISA User's Guide

**Supplied with Agilent Command Modules , Embedded Controllers, and VXLink.*

Contents

Chapter 4
Using the Universal Instrument Driver

Chapter 5
Example Programs using SCPI

Chapter 6
Firmware Upgrade Utility

Legal and Safety Information

Chapter 1
Installation

Product Overview

The SpectralBER 10 Gb/s System comprises:

- Agilent VXI C-Size Mainframe.
- Agilent E1406A Command Module.
- Agilent J1421A Clock Source Module
- Agilent HP J1421B Transmitter Module and/or J1420B Receiver Modules in any combination
- Optionally an Agilent J1426A 2 MHz (MTS) or Agilent J1427A 1.5 Mb/s (BITS) Reference Clock Module.

It can be controlled from a PC or workstation using any of the following:

- SCPI Commands.
- Universal Instrument Drivers.
- A Soft Front Panel.

Note **Installation is performed in the following order:**

1 Prepare

1.1 Initial Inspection

Inspect the shipping containers for damage. If the shipping containers or cushioning material is damaged, it should be kept until the contents of the shipment have been checked for completeness and the system has been checked both mechanically and electrically. Procedures for checking electrical operation are given in the individual module User's Manuals. If the contents of the shipment are incomplete, if there is mechanical damage or defect, notify the nearest Agilent Office. If the system does not pass the electrical performance tests given in the individual module User's Manual, notify the nearest Agilent office. If the shipping container is also damaged, or the cushioning material shows signs of stress, notify the carrier as well as the nearest Agilent office. Keep the shipping materials for the carrier's inspection. The Agilent office will arrange for repair or replacement without waiting for claim settlement.

WARNING **TO AVOID HAZARDOUS ELECTRICAL SHOCK, DO NOT PERFORM ELECTRICAL TESTS WHEN THERE ARE SIGNS OF SHIPPING DAMAGE TO ANY PORTION OF THE OUTER ENCLOSURE (COVERS, PANELS, METERS).**

1.2 Operating Environment

This system is designed for indoor use only. **DO NOT** operate the product in an explosive atmosphere or in the presence of flammable gases or fumes. The system may be operated in environments within the following limits:

Temperature +5 ^{o}C to +35 ^{o}C

Altitude up to 3050 m (10,000 ft).

Humidity 30% to 85% relative humidity to 40 ^{o}C.

The system should be protected from temperature extremes which may cause condensation.

Caution

The module is designed for use in Installation Category II and Pollution Degree 2 per IEC 61010 and 644 respectively.

1.3 Power Requirements

The mainframe can be operated at line voltages of 90 VAC to 264 VAC, and line frequencies of 47 Hz to 66 Hz. The mainframe can also operate at 360 Hz to 440 Hz with line voltages of 90 VAC to 132 VAC.

The mainframe ships with a power cord and with a fast blow fuse installed. The fuse is suitable for all line voltages. The fuse is not user replaceable. Refer to "Replacement Power Cords" on page 215 of the *E8404A VXI C-Size Mainframe User and Service Manual* for additional information on power cords and on fuse replacement. Appendix A contains complete input power specifications.

WARNING

WARNING The power cord is the only way to disconnect the mainframe from AC power and, therefore, it must be accessible to the operator at all times. When the mainframe is mounted in a system cabinet, the power cord need not be accessible since the cabinet must have its own disconnect device.

Module Power Requirements

VXI modules are powered from the VXI Mainframe. The mainframe provides adequate power for all the SpectralBER modules.

1.4 Cooling

The mainframe provides adequate cooling for SpectralBER modules.

Positioning the Mainframe for Adequate Cooling

VXI instruments are cooled by air drawn through the back of the mainframe and exhausted out the sides. The power supply is cooled by air drawn from the right side (facing the mainframe) and exhausted out the left side. When placing the mainframe on a work bench or if the mainframe is rack mounted, provide at least a one inch clearance at the back and sides to allow for proper air flow.

Caution

Do not restrict the air flow into or out of the VXI Mainframe.

2 Install Hardware

2.1 Installing a Mainframe

If the VXI Mainframe(s) are to be installed in a system cabinet (rack mounted) do this first using the instructions supplied with the system cabinet before installing the modules. Otherwise place the VXI Mainframe(s) on a suitable table or bench before installing the modules.

Note Set the module address switches as appropriate before installing the modules. Refer to the following paragraphs for details.

2.2 Setting Module Addresses

A SpectralBER 10 Gb/s System is a “virtual instrument” in VXI terms, consisting of up to 4 message based servants. The servants can be any mix of Clock Source, Transmitters and/or Receivers.

Note The Timing Sources (J1426A and J1427A) if used are NOT part of the VXI instrument. They only take power from the VXI bus backplane.

To create the VXI instrument, the normal VXI rules as regards logical address settings must be observed. Each servant Clock Source, Transmitter and/or Receiver must have its logical address set such that it is unique within the VXI Mainframe and within the servant area setting of the Slot 0 Command Module. The logical addresses of the servant modules are set by switches on the modules. (Refer to the following paragraphs for details.) A typical configuration using the factory default settings is shown in Table 1-1 which corresponds to the system shown in Figure 1-2.

Table 1-1. A Typical SpectralBER 10 Gb/s Configuration

VXI Slot	Module	Logical Address	Servant Area	GPIB Address
0	E1406A Command Module	0*	255*	70900
2	J1426A Timing Source	---**	---	---**
3/4	J1421A Clock Source	16*	---	70902
5/6/7	J1422B Transmitter	24*	---	70903
8/9/10	J1420B Receiver	32*	---	70904

* *Factory Default Setting*

** *The Timing source is not part of the VXI instrument. Only power is supplied from the VXI bus backplane. No control is needed.*

E1406A Command Module

In general, you will not need to change the Command Module switches from their default settings.If you do need to change the settings for your system, see the *E1406A Command Module User’s Manual* for details.

Note Install the E1406A Command Module in Slot 0. See Figure 1-2.

J1421A Clock Source

In general, you will not need to change the Clock Source Logical Address switches from their default setting (logical address 16 / GPIB secondary address 01). If you do need to change the setting for your system, assign a logical address to the Clock Source module by setting the Logical Address switches on the rear panel of the module (their position is indicated on the side cover of the module, see Figure 1-1). The setting selected must not conflict with the logical address of any other module in the system.

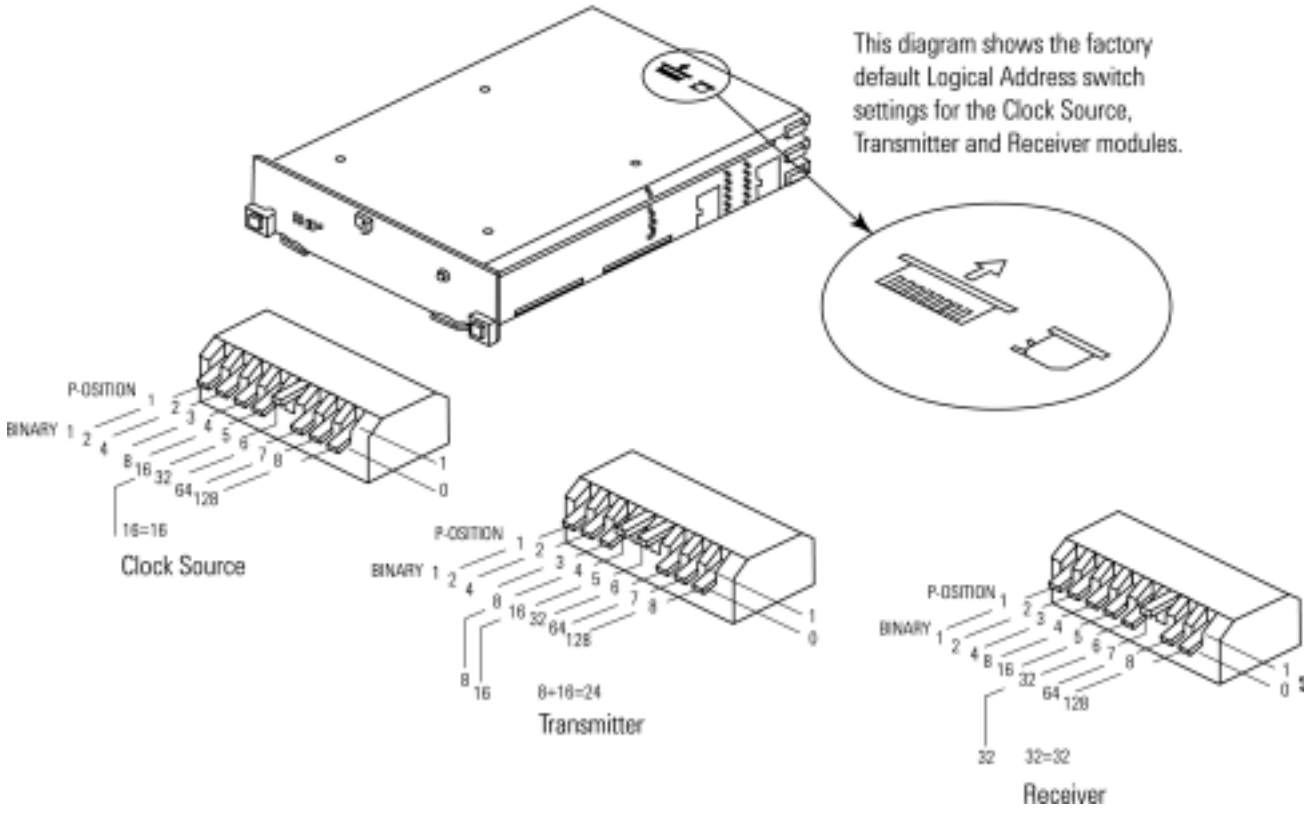


Figure 1-1. Setting the Logical Address Switches

J1422B Transmitter

In general, you will not need to change the Transmitter Logical Address switches from their default setting (logical address 24 / GPIB secondary address 02) unless you are installing more than one Transmitter module in a mainframe. If you do need to change the setting for your system, assign a logical address to the Transmitter module by setting the Logical Address switches on the rear panel of the module (their position is indicated on the side cover of the module, see Figure 1-1). The setting selected must not conflict with the logical address of any other module in the system.

J1420B Receiver

In general, you will not need to change the Receiver Logical Address switches from their default setting (logical address 32 / GPIB secondary address 03) unless you are installing more than one Receiver module in a mainframe. If you do need to change the setting for your system, assign a logical address to the Receiver module by setting the Logical Address switches on the rear panel of the module (their position is indicated on the side cover of the module, see Figure 1-1). The setting selected must not conflict with the logical address of any other module in the system.

J1426A/J1427A Timing Sources

The Timing Sources J1426A 2MHz MTS or J1427A 1.5 MB/s BITS if used, are not GPIB modules and so have no Logical Address switches.They only take power from the VXI bus backplane.

2.3 Positioning the Modules

The E8404A Mainframe supplied has 13 slots, with the exception of the E1406A Command Module (Slot 0 Controller) which must be positioned in Slot 0, the SpectralBER modules can be loaded in any of the remaining 12 slots in the mainframe. However, we recommended that modules be loaded in the order shown in Figure 1-2 to facilitate connecting the modules using the semi rigid cables provided to connect the Clock Source to the Transmitter Module and the Receiver Module to the Clock Source. Each Transmitter and Receiver module occupies 3 VXI slots, the Clock Source Module occupies 2 slots and the Timing Source Module one slot. In one mainframe therefore, one Timing Source, one Clock Source, one Transmitter and two Receiver modules can be accommodated. If Receiver Modules only are required in a mainframe then four can be accommodated.

Note

To be EMC compliant, all unused slots in the VXI Mainframe must be covered with an EMC Filler Panel (Agilent Part No. E8400-60202) supplied with the system.

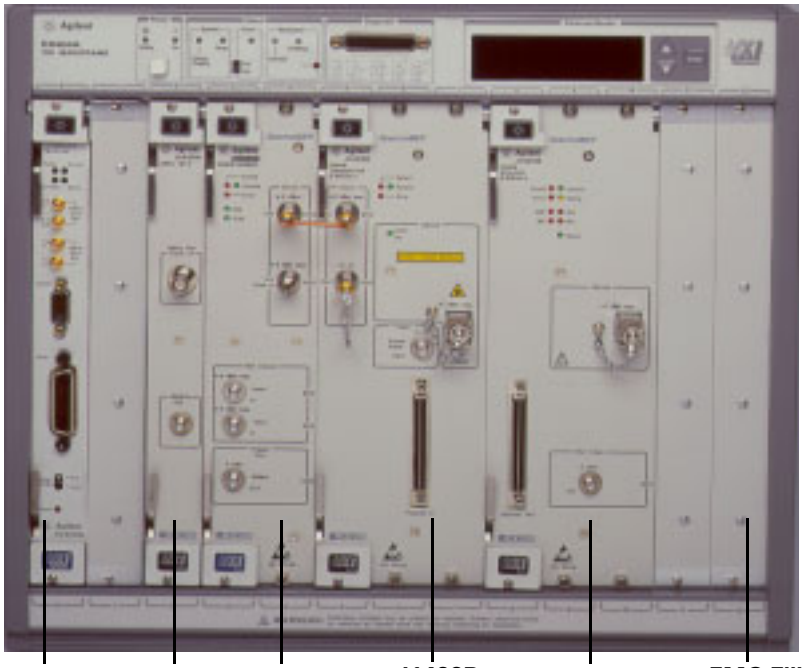


Figure 1-2. Module Positions

2.4 Installing Modules

Caution **Disconnect power from the mainframe before inserting or removing modules to prevent irreparable damage to the module or mainframe.**

Install the modules in their respective slots using the procedure in Figure 1-3.

Note All modules in the mainframe are grounded through the mainframe chassis. During installation, tighten the instrument's retaining screws (Step 4) to secure the instrument to the mainframe and to make the ground connection.

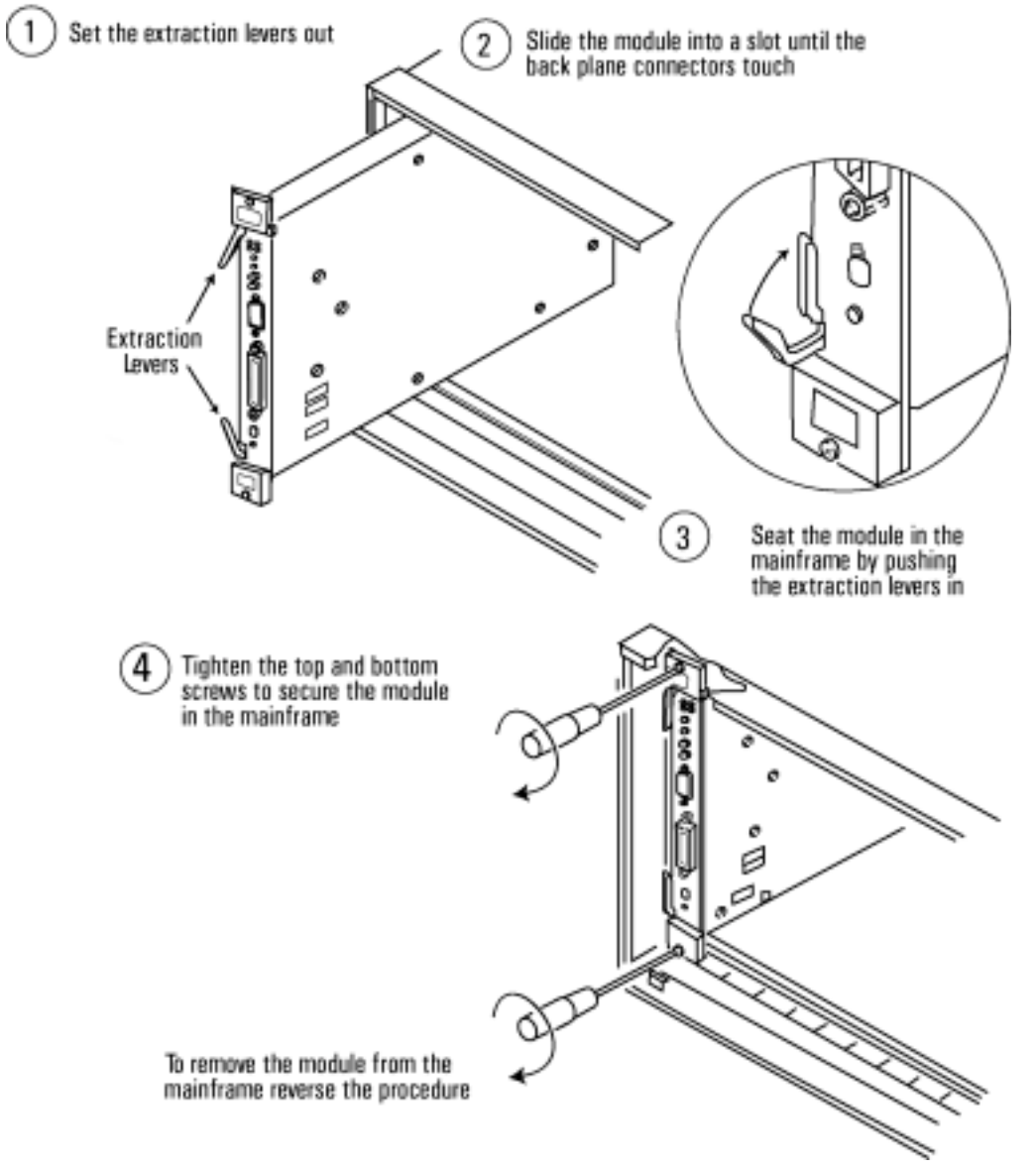


Figure 1-3. Installing a Module in a VXI Mainframe

3 Power On Check

1. Switch on the VXI mainframe and check that the mainframe powers up and that the fans operate.

2. Check the Command Module LEDs. **Failed** will turn ON then OFF, **Access** will be flashing and **Ready** will be ON.

3. Check the Clock Source LEDs. **Failed** will turn ON then OFF, **Access** will be flashing and **10G** will be ON.

4. Check the Transmitter LEDs. **Failed** will turn ON then OFF and **Access** will be flashing.

5. Check the Receiver LEDs. **Failed** will turn ON then OFF, **Access** will be flashing and **OOF** will be ON.

4 Install GPIB

The SpectralBER system requires an external controller (PC or Workstation) fitted with a GPIB interface. If you have not already done so, install a GPIB interface card and it's associated software in your external controller.

The following paragraphs describe installing an Agilent GPIB Interface. If installing any other manufacturer's GPIB Interface follow the installation instructions supplied with that interface.

Note These components are not supplied with SpectralBER.

4.1 Install GPIB Interface

Install a GPIB Interface in your external controller. (See the *GPIB Interface Installation Guide* supplied with the interface for instructions.)

4.2 Install I/O Libraries

Install the I/O Libraries supplied with the GPIB interface in your external controller. (See the *I/O Libraries Installation and Configuration Guide* supplied with the interface for instructions.)

4.3 Configure I/O Libraries

If the I/O Config utility was not automatically run at the end of the installation process, run it now using the instructions in *I/O Libraries Installation and Configuration Guide* supplied with the interface.

1. Launch the I/O Config utility that comes with the I/O Libraries.

2. In the **Available Interface Types** window, select VXI Command Module and press **Configure**. (The default VISA Interface Name should be acceptable.)

3. It is likely that you will only have one GPIB card in your controller, in which case you should choose GPIB0. If you have more than one card, ensure that you choose whichever one your mainframe is connected to.

4. The GPIB Primary address can be found by looking at the DIP switches on the Command Module. Each Command Module must have a unique address (the default is 9) to allow it to be identified on the GPIB bus.

5. Press **OK** and you will see the new interface added to the list of interfaces.

Note Late information about configuring a SpectralBER system will be found on the SpectralBER System Software CD in the *readme* file.

5 Install Software

Description

SpectralBER system software is supplied on a CD. The software supports Windows95/98/NT/2000. For each system it comprises:

- Instrument Firmware
- Universal Instrument Driver
- Soft Front Panel
- Firmware Upgrade Utility

Instrument Firmware

The Instrument Firmware is the SpectralBER code installed in the individual Clock Source, Transmitter and Receiver modules.

Universal Instrument Driver

The Universal Instrument Driver (UID) is built on top of, and uses the services provided by VISA (Virtual Instrument Software Architechture). (VISA is installed with the I/O Libraries, see 4 Install GPIB on page 12.) The driver can be used with any GPIB Interface for which the manufacturer has provided a VISA DLL. It includes a "Function Panel" (.fp) file which allows it to be used with visual programming environments such as HP-VEE, LabWindows, and LabVIEW.

Soft Front Panel

The Soft Front Panel provides a graphical user interface for the SpectralBER system. It is also used to verify system communications and functionality when the system is first installed and can be used as a learning tool to demonstrate system control and capability. It is also a useful tool for debugging software under development.

Firmware Upgrade Utility

The Firmware Upgrade Utility is provided so that you can easily upgrade the instrument firmware.

Platforms & Operating Systems

SpectralBER is compatible with; WIN95/98, WINNT 4.0, WIN2000 and SUN.

Hardware Requirements (Windows Platforms)

When running SpectralBER software under Microsoft Windows, the following hardware is recommended:

- Pentium or higher processor.
- 16 MB RAM minimum, 32 MB RAM recommended (Windows 95/98).
- 32 MB RAM minimum, 64 MB RAM recommended (Windows NT/2000).
- 20 MB free hard disk space.
- CD-ROM drive.
- 1024 x 768 pixel 256-color display or better.
- GPIB card that supports Microsoft Windows 95/98/NT/2000.

Other Software Requirements

- I_O Libraries for Instrument Control (VISA and SICL), supplied with your GPIB Interface.
- Any other application programs such as C or C++ that you wish to use to program the VXI system.

5.1 Install I/O Libraries

If you have not already done so, install the software (VISA and SICL) using the media and instructions supplied with your GPIB Interface card. See 4 Install GPIB on page 12.

5.2 Install SpectralBER System Software

SpectralBER System Software is on the CD supplied with your SpectralBER System. The CD has four directories, two that correspond to the platforms supported:

- Windows 95/98/2000/NT
- Solaris

The two other directories on the CD contain:

- Manuals (in *pdf* format)
- Adobe Acrobat Reader (required to read the *pdf* files)

The two platform directories each contain the System Software appropriate to the particular platform.

Windows 95/98/2000/NT

The System Software for Windows 95/98/NT/2000 consists of:

- Universal Instrument Driver (UID)
- SpectralBER soft front panel
- SpectralBER Upgrade Utility
- SpectralBER Instrument Firmware

Install SpectralBER System Software for Windows 95/98/2000/NT

1. Insert the CD in your drive, the CD should auto run.
2. Follow the instructions on the screen to install the software.

Note The installation automatically installs a run-time version of LabWindows[1].

If the CD does not auto run:

1. Using MS Explorer access the *win95nt* directory on the CD.
2. Read the *Readme* file.
3. Run the *setup* file to install the System Software.

1. LabWindows is a product of National Instruments Corporation.

Solaris The System Software for Solaris consists of:

- Universal Instrument Driver (UID)
- SpectralBER soft front panel
- SpectralBER Upgrade Utility
- SpectralBER Instrument Firmware

Install SpectralBER System Software for Solaris

Note Root permissions are required to install the driver.

From the *solaris/driver* directory on the CD:

1. Read the *Readme* file.
2. Copy the *hp142xb_pkg.tar* file to */tmp*.
3. cd to */tmp*.
4. *tar -xvf ./hp422xa_pkg.tar*
   or
   tar -xvf ./hp142xb_pkg.tar
5. After the package has been extracted, install it with the command *pkgadd -d /tmp/hp142xb_pkg*

Note: Uninstall facilities are also provided.

From the *solaris/panel* directory on the CD:

6. Read the *Readme* file.
7. *./install.*
8. Follow the on screen instructions.

Note The installation automatically installs a run-time version of LabWindows[1].

5.3 Install Application Programs

If you have not already done so, install the application programs to program the VXI system, such as C, C++ for example, according to the instructions supplied with the software.

1. LabWindows is a product of National Instruments Corporation.

6 Verify

You can verify both hardware and software installation by starting the Soft Front Panel. (Soft front panel software was installed as part of “Install SpectralBER System Software” on page 14.)

6.1 Start the Soft Front Panel

Windows 95/98/NT/2000 In the directory *C:\Vxipnp\winNT(win95/98)\10GSpectralBER* double click on the file *10G.exe*, or double click on the application icon.

Solaris Execute the command *10G.exe*.

1. The Instrument Detect window shown in Figure 1-4 will be displayed.:

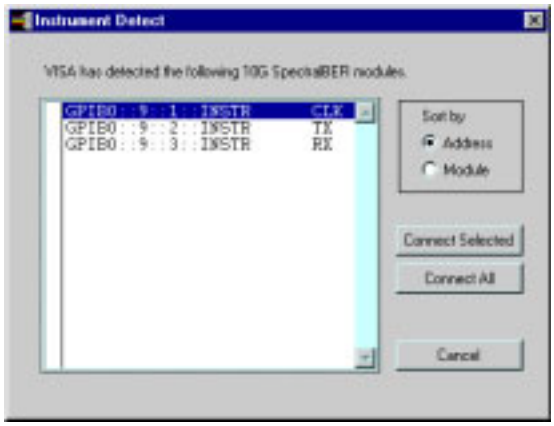


Figure 1-4. Instrument Detect Window

Note

In this case VISA has detected three SpectralBER modules:
GPIB0::9::1::INSTR
GPIB0::9::2::INSTR
GPIB0::9::3::INSTR
which means that at least three modules with GPIB Secondary addresses of 1, 2 and 3 respectively have been correctly installed.

2. Either select one of the modules and click on **Connect Selected**, or click on **Connect All** to start the Soft Front Panel. Figure 1-5 below shows a typical Soft Front Panel.

Figure 1-5. A Typical Soft Front Panel

7 Connect

Caution

Damage can occur to the optical input port of the J1420B if it is connected directly to the optical output port of the J1422B.

Damage can occur to optical input ports if power exceeds 0 dBm.

If a module is not used as specified, the protection provided by the equipment could be impaired. The module must be used in a normal condition only (in which all means for protection are intact).

Before connecting or disconnecting, ensure that you are grounded, or make contact with the metal surface of the VXI Mainframe with your free hand to bring you, the module, and the mainframe to the same static potential. Modules remain susceptible to ESD damage while the module is installed in the VXI Mainframe.

Additional ESD information is required when servicing see "ESD Precautions" in the module manuals.

7.1 Clock Source toTransmitter

Connect the Clock Source and Transmitter modules as described below

Electrical Connections

The J1422B Transmitter Module does not have an internal clock generator. Connect one of the Timing Source modules (J1426A or J1427A if required) to the J1421A Clock Source Module and the J1422B Transmitter as follows:

1. Connect the source clock (MTS or BITS) to the Timing Source module (**Ref In**).

2. Connect the Timing Source module (**Clock Out**) to the Clock Source module (**Ref Clock In Insert**). Use the semi rigid cable provided as shown in Figure 1-6.

3. Connect the Clock Source module (**Clock Out**) to the J1422B Transmitter Module (**Clock In**). Use the semi rigid cable provided as shown in Figure 1-6.

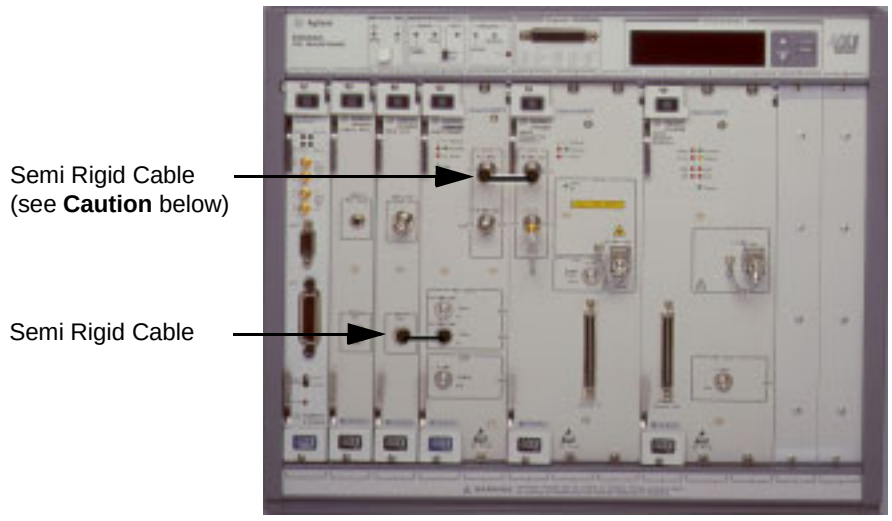


Figure 1-6. Clock Source toTransmitter Electrical Connections

Caution **Use the cable provided to connect the J1421A Clock Source and J1422B Transmitter modules. The line clock signal from the Clock Source is at 10 GHz.**

Note Optimum performance of Precision 3.5 mm connectors is achieved when they are tightened to a torque of 90 Ncm (5 lb-inch).

Optical Connection

Caution **Damage can occur to the Optical Input port of a J1420B Receiver if it is connected directly to the Optical Output port of a J1422B Transmitter. (Damage can occur if input power exceeds 0 dBm.)**

Connect the optical cable to the Transmitter **Optical Out** connector, connect the other end of the optical cable to the Receiver **Optical In** connector or to the device to be tested.

7.2 Receiver to Clock Source

To synchronize the Transmitter module to received data, connect the Clock Source and Receiver modules as described below .

Electrical Connection - Loop Timing (Synchronizing with Received Data)

1. Connect the J1421A Clock Source Module (Clock Out) to the J1422B Transmitter Module (Clock In). Use the semi rigid cable provided as shown in Figure 1-7.

2. Connect the Ref Clock Out of the J1420B Receiver Module to the Ref Clock In Slave of the J1421A Clock Source Module as shown in Figure 1-7.

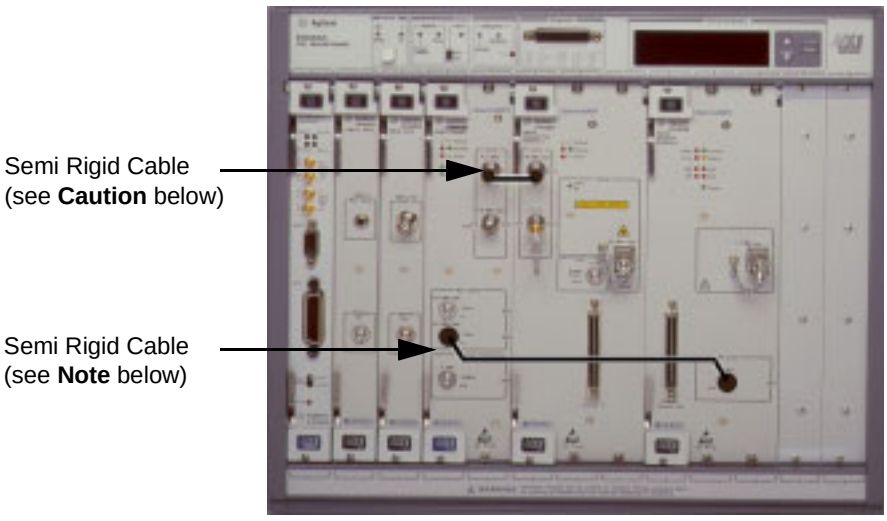


Figure 1-7. Receiver to Clock Source Electrical Connections

Caution **Use only the cable provided to connect the J1421A Clock Source and J1422B Transmitter modules. The line clock signal provided by the Clock Source is at 10 GHz.**

Note Use of the supplied semi rigid cable between the J1420B Receiver and the J1421A Clock Source is only possible when the Clock Source, Transmitter and Receiver are next to each other in the same VXI Mainframe. If this is not the case, use a suitable flexible cable instead.

Note Optimum performance of Precision 3.5 mm connectors is achieved when they are tightened to a torque of 90 Ncm (5 lb-inch).

Optical Connection

Caution **Damage can occur to the Optical Input port of a J1420B Receiver if it is connected directly to the Optical Output port of a J1422B Transmitter. (Damage can occur if input power exceeds 0 dBm.)**

Connect the optical cable to the Transmitter **Optical Out** connector; connect the other end of the optical cable to the Receiver **Optical In** connector or to the device to be tested.

Chapter 2
SpectralBER Overview

This chapter contains general information on the composition of the Agilent SpectralBER 10 Gb/s System.

It uses the E8404A C-Size Mainframe with enhanced monitoring capabilities. The enhanced monitoring capabilities allow you to monitor power supply voltages, mainframe temperatures, fan operation and backplane operation. Refer to the *VXI C-Size Mainframe User and Service Manual* for specific details of the mainframe.

Product Overview

The 10 Gb/s System comprises:

- Agilent VXI C-Size Mainframe.
- Agilent E1406A Command Module.
- Agilent J1421A Clock Source Module
- Agilent J1422B Transmitter Module and/or J1420B Receiver Modules in any combination
- Optionally an Agilent J1426A 2 MHz (MTS) or Agilent J1427A 1.5 Mb/s (BITS) Reference Clock Module.

The system can be controlled from a PC or workstation using any of the following:

- SCPI Commands
- Universal Instrument Drivers
- A Soft Front Panel

In a 10 Gb/s System each VXI mainframe needs a Command Module to provide the required control of the message-based Transmitter/Receiver modules.

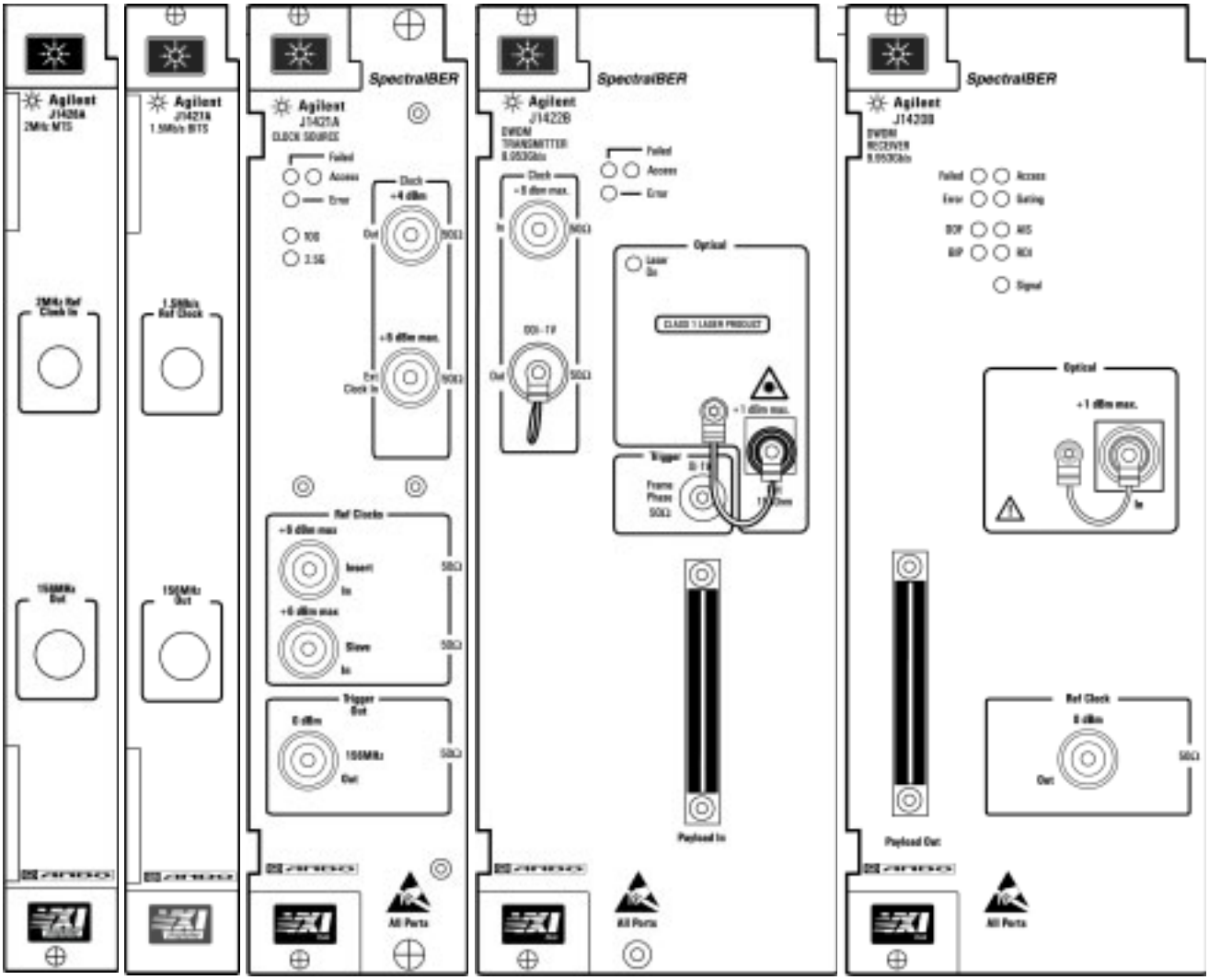
Each Transmitter and Receiver module occupies 3 VXI slots, the Clock Source Module occupies 2 slots and the Reference Clock Module one slot. In one 13 slot C-Size VXI Mainframe therefore, one Clock Source, one Clock Reference, one Transmitter and two Receiver modules can be accommodated. If Receiver Modules only are required in a mainframe then four can be accommodated.

Note To be EMC compliant, all unused slots in the VXI Mainframe must be filled with an EMC Filler Panel (Agilent Part No. E8400-60202).

VXI Mainframe & Command Module

Details of the VXI Mainframe and the Command Module are in the manuals suppled with those components. (Refer to the *VXI C-Size Mainframe User and Service Manual* and the *Command Module Users Manual)*.Controller to Module Communication

To communicate with modules, SCPI commands are sent from the external controller to the Command Module (Slot 0 Controller) in slot 0. The commands are passed by the Command Module directly to individual modules.



Typical 10 Gb/s System Modules

SpectralBER Modules

Receiver Module (J1420B)

The Agilent J1420B is a message-based C-size three slot VXI module. It is the Receiver Module of the 10 Gb/s System and is used in combination with an Agilent J1421A Clock Source Module and Agilent J1422B Transmitter Module(s).

In a 10 Gb/s signal carrying PRBS payloads it makes BER measurements, captures J0/J1 trace messages, detects B1, B2, B3, REI-L/MS-REI, REI-P/HP-REI and Bit errors and alarms as listed below:

- LOS
- OOF
- LOF
- AIS-L/MS-AIS
- RDI-L/MS-RDI
- AIS-P/AU-AIS
- LOP-P/AU-LOP
- RDI-P/HP-RDI

For more information about this module, see the appropriate *Receiver Module User's Manual* and the *Specification* document supplied in the *System Manuals* Binder.

Clock Source Module (J1421A)

The Agilent J1421A is a message based C-size double-slot VXI module. It is the Clock Source Module of the 10 Gb/s System and is used in combination with Agilent J1422B Transmitter Module(s) and Agilent J1420B Receiver Module(s).

It supplies a clock signal at 10 Gb/s (and optionally 2.5 Gb/s) for the J1422B Transmitter Module. The Clock Source can be synchronized to an external 10 Gb/s (and optionally 2.5 Gb/s) clock or alternatively to a reference clock at either 2.5 GHz, 622 MHz or 156 MHz.

For more information about this module, see the *Clock Source/MTS/BITS and Transmitter Module User's Manual* and the *Specification* document supplied in the *System Manuals* Binder.

Reference Clock Source (J1426A/J1427A)

The Agilent J1426A and J1427A are single-slot VXI modules. They provide a 155.52 MHz Reference Clock Insert for the J1421A Clock Source from a 2 MHz MTS (J1426A) or a 1.5 Mb/s BITS (J1427A) clock input.

For more information about this module, refer to the *Clock Source/MTS/BITS and Transmitter Module User's Manual* and the *Specification* document supplied in the *System Manuals* Binder.

Transmitter Module (J1422B)

The Agilent J1422B is a message based C-size double-slot VXI module. It is the Transmitter Module of the 10 Gb/s System and is used in combination with Agilent J1421A Clock Source Module and Agilent J1420B Receiver Module(s).

It has the following characteristics:

- ITU-T 1550 nm wavelength optical output.
- Transmits SDH/SONET STM-64/OC-192 framed signals.
- Concatenated payloads, channelized payloads down to VC-3/STS-1.
- Error injection.
- Alarm generation.
- Pointer control.

- Generates J0/J1 trace messages.
- APS control.
- Signal and path overhead edit.

For more information about this module, refer to the *Clock Source/MTS/BITS and Transmitter Module User's Manual* and the *Specification* document supplied in the *System Manuals* Binder.

Chapter 3
The Soft Front Panel (GUI)

Introduction

The Agilent SpectralBER system can be controlled from a PC or workstation using either SCPI commands, Universal Instrument Drivers or manually using the Soft Front Panel (Graphical User Interface). This chapter describes using the Soft Front Panel.

For more information on using SCPI commands, see Example Programs using SCPI on page 57 and the *SpectralBER System (10 Gb/s) Remote Control Manual*. For more information on the Universal Instrument Drivers, see Using the Universal Instrument Driver on page 49.

The Soft Front Panel provides a graphical user interface for the SpectralBER System. As well as being another method of controlling the system, it is used to verify system communications and functionality when the system is first installed, see 6 “Verify” on page 16. It can also be used as a learning tool to demonstrate system control and capability.

In addition, it is a useful tool for debugging software under development. For example, the soft front panel can interrogate the system for its current status. The modules are not forced to defined states before displaying the current system status such as module states, number of modules, and their logical addresses etc.

Starting the Soft Front Panel

Windows 95/98/NT/2000 In the directory *C:\Vxipnp\winNT(win95/98)\10GSpectralBER* double click on the file *10G.exe*, or double click on the application icon.

Solaris Execute the command *10Gspectralber_soft_panel.*

SpectralBER 10 Gb/s System

1. The Instrument Detect window shown in Figure 3-1 will be displayed.:

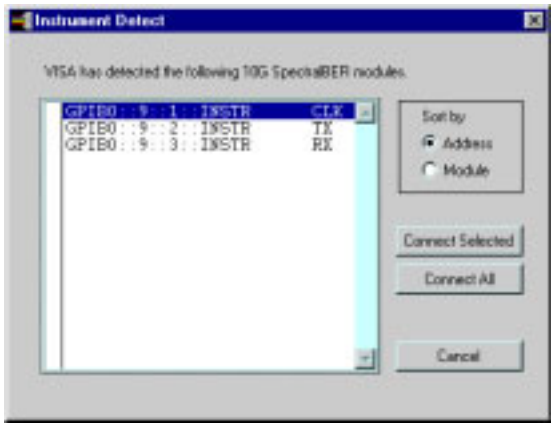


Figure 3-1. Instrument Detect Window

Note In this case VISA has detected three 10G SpectralBER modules:

GPIB0::9::1::INSTR
GPIB0::9::2::INSTR
GPIB0::9::3::INSTR

which means that three modules with GPIB Secondary addresses of 1, 2 and 3 respectively have been correctly installed.

2. Either select any combination of the modules detected and click on Connect Selected, or click Connect All to start the Soft Front Panel.

Soft Front Panel Description

Figure 3-2 illustrates a typical SpectralBER 10 Gb/s System Soft Front Panel and it's main features. It is divided into four areas; Transmitter Setup, Receiver Setup, Clock Setup and Results. Each page of results contains four separate Results Panels. One Results Panel is highlighted for each Receiver in the system (identified by the GPIB address at the top of the panel). If the system contains more than four Receivers, click on the page Down button at the right hand side of the page to display the next four Receiver Results panels. The following pages describe the four areas in more detail.

Note The Soft Front Panel has been optimized for use at a screen resolution of 1024 by 768 pixels. A lesser resolution may detract from the usability.

Any change to the soft front panel is actioned immediately. Changing the value of a field automatically changes the instrument settings.

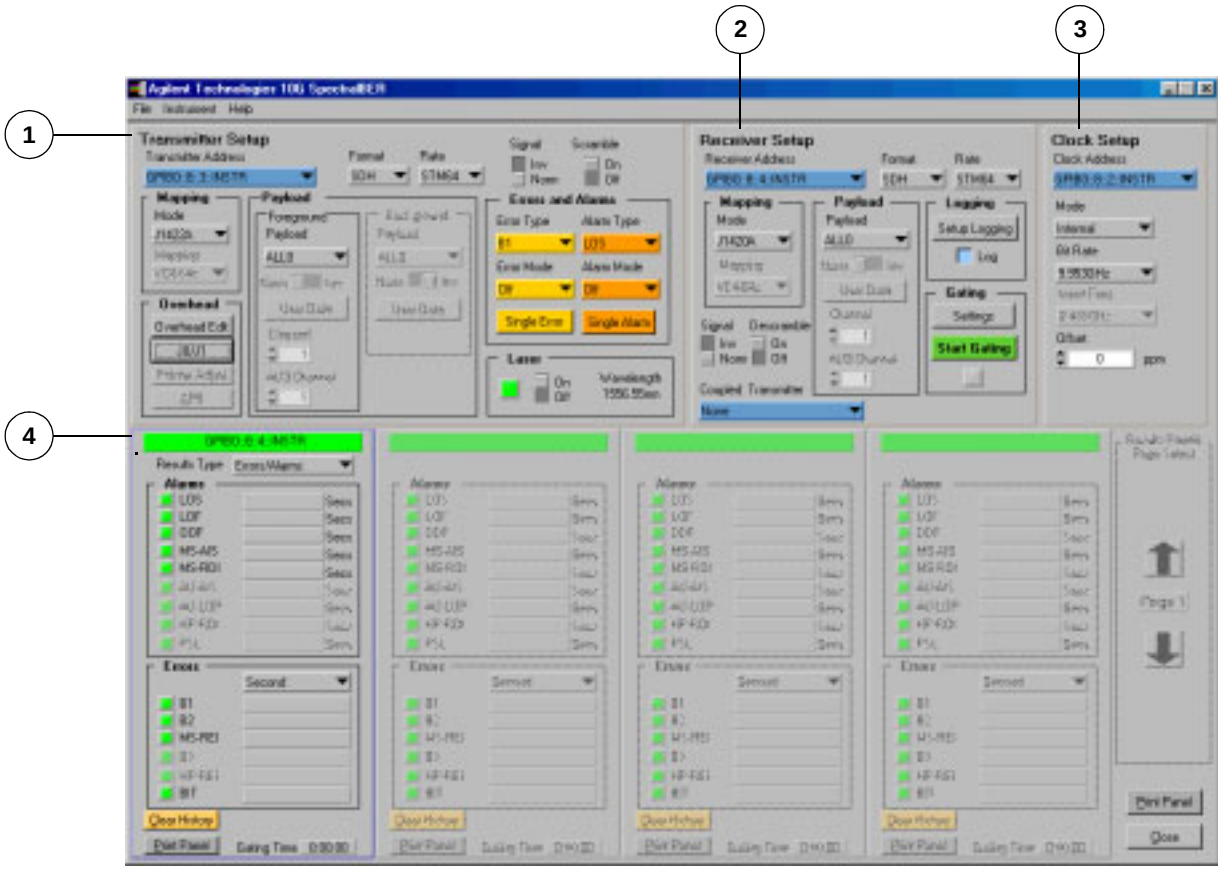


Figure 3-2. A Typical 10 Gb/s System Soft Front Panel

1 Transmitter Setup, see Figure 3-3.

2 Receiver Setup, see Figure 3-10.

3 Clock Setup, see Figure 3-14.

4 Results Display, see Figure 3-15.

Transmitter Setup

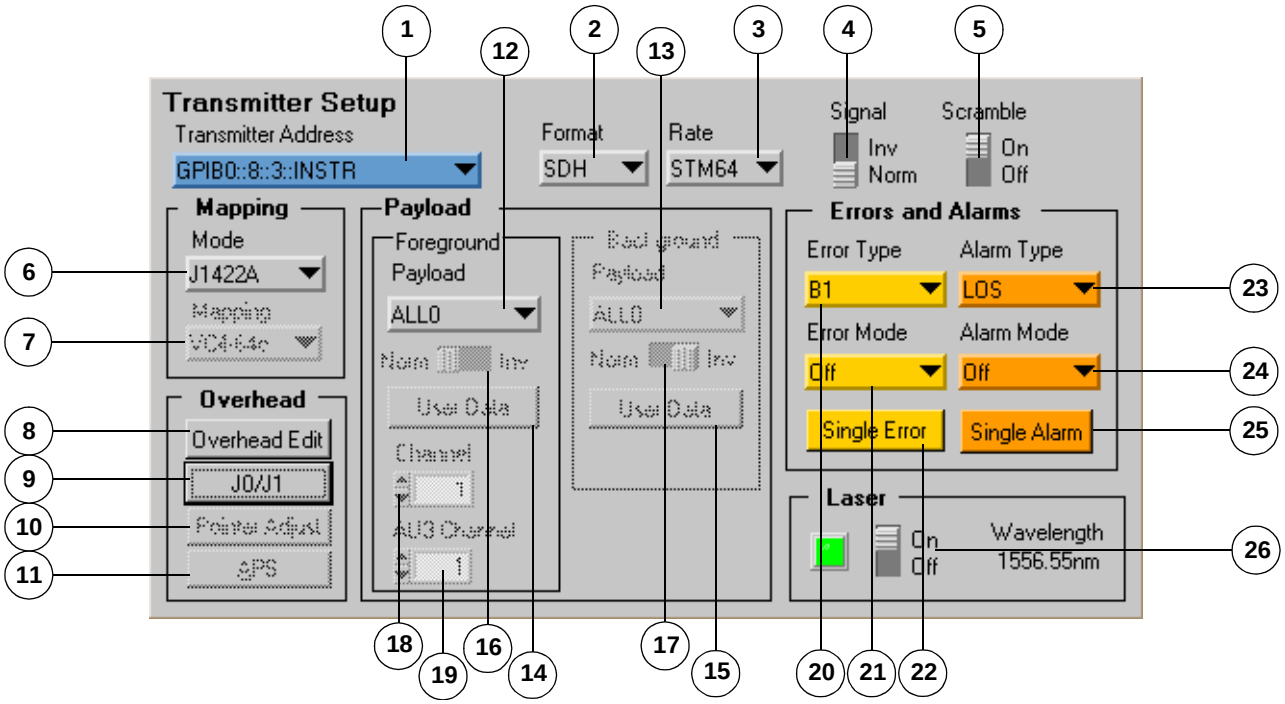


Figure 3-3. Transmitter Setup Area

1 Select a transmitter module.

2 Select the framing format.

3 Select the transmission rate*.

4 Invert the signal.

5 Scramble the frame.

6 Select the mapping mode.

7 Select the mapping.

8 Edit the overhead, see Figure 3-4.

9 Edit the J0/J1 string, see Figure 3-5.

10 Adjust the pointer, see Figure 3-6.

11 Setup APS settings, see Figure 3-7.

12 Select the foreground payload.

13 Select the background payload.

14 Edit the foreground user pattern when the foreground payload **(12)** is set to User, see Figure 3-8.

15 Edit the background user pattern when the background payload **(13)** is set to User, see Figure 3-9.

16 Invert the foreground pattern.

17 Invert the background pattern.

18 Select the foreground payload channel. The channel selection range depends on the mapping selected **(7)**.

19 Select the foreground payload AU3/STS1 channel when the foreground payload **(12)** is set to VC3/STS-1.

20 Select the error type.

21 Select the error mode.

22 Inject a single error.

23 Select the alarm type.

24 Select the alarm mode†.

25 Inject a single alarm.

26 Switch the laser on/off.

---

* When changing rate, remember to also change the Bit Rate on the Clock Source, see Figure 3-14.

† The repeat alarm mode can be used to stress the boundary conditions for alarm detection. To permit this the Repeat alarm mode generates the condition that will cause the alarm for the number of frames requested.

Overhead Edit

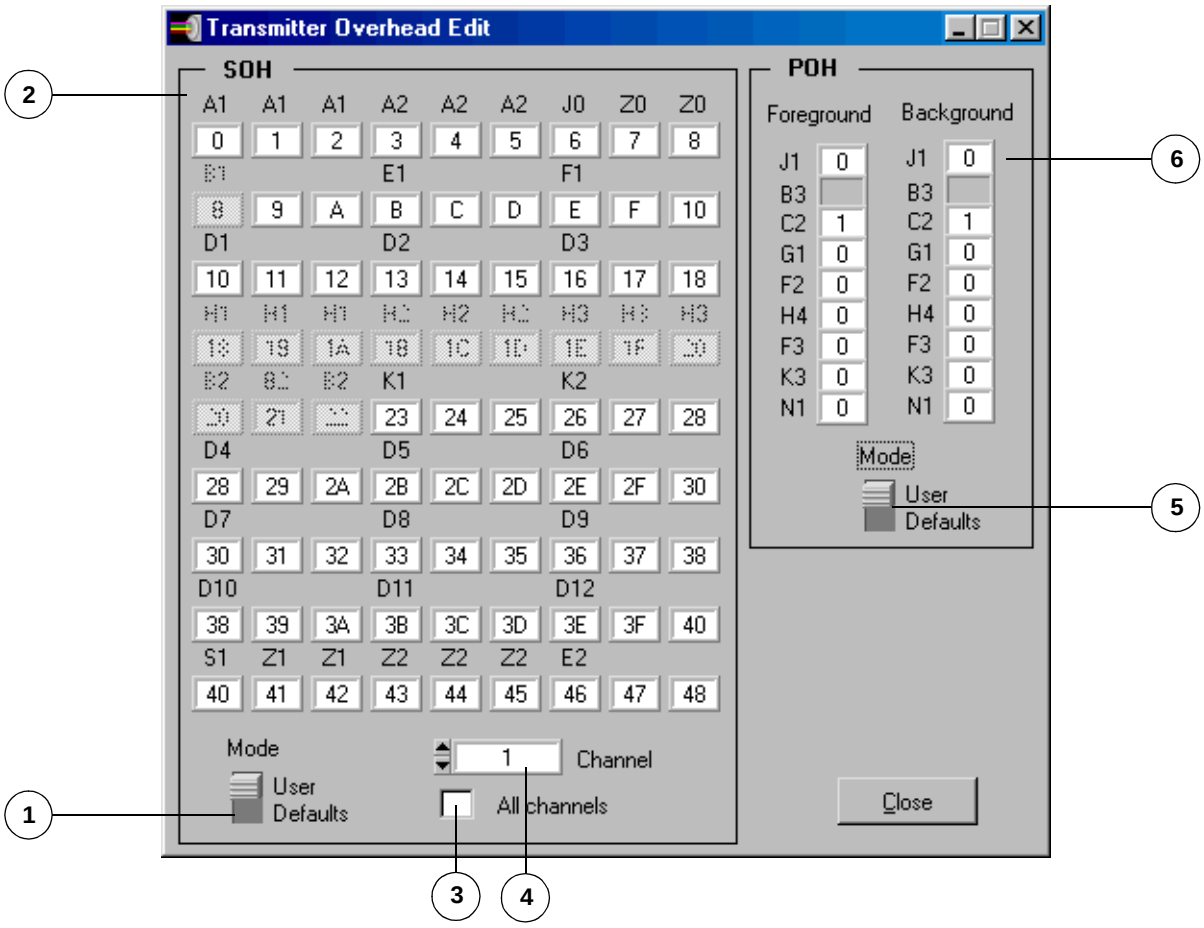


Figure 3-4. Transmitter Overhead Edit

Section/TOH Overhead

1 Set to user editable or default settings.

2 User editable bytes.

3 Select all channels.

4 Select a channel.

Path Overhead

5 Set to user editable or default settings.

6 User editable bytes.

J0/J1 Messages

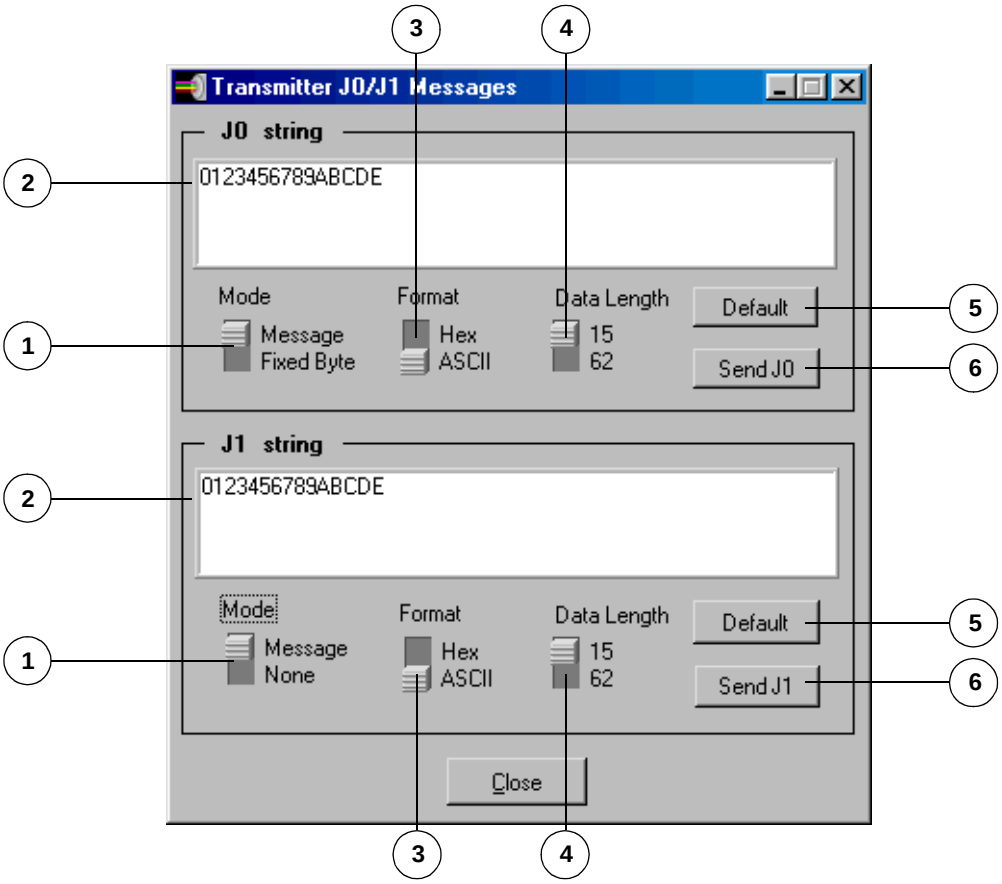


Figure 3-5. Transmitter J0/J1 Message Setting

J0 string & J1 string

1 Set the message mode.

2 String edit area.

3 Set the string format to ASCII or Hex.

4 Set the length of the data string to 15 or 62* when in ASCII mode or to 16 or 64* when in Hex mode.

5 Select the default string.

6 Send the string.

* When the string format is set to ASCII and the data length to 15, CRC is calculated and added to the transmitted string. When the string format is set to ASCII and the data length to 62, CR+LF is added to the transmitted string. When the string format is set to Hex and the data length to either 16 or 64, the string is sent as specified with no addition.

Pointer Adjust

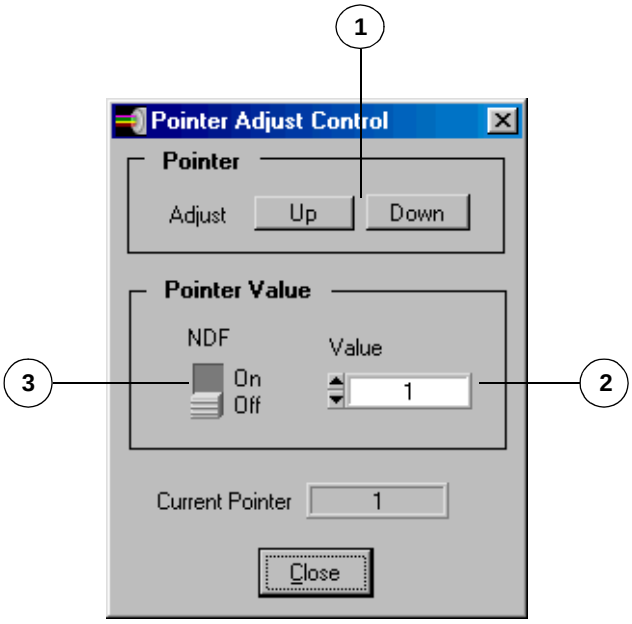


Figure 3-6. Pointer Adjust Control

1 Adjust the pointer up or down.

2 Adjust the pointer value.

3 Set new data flags on or off.

APS Setting

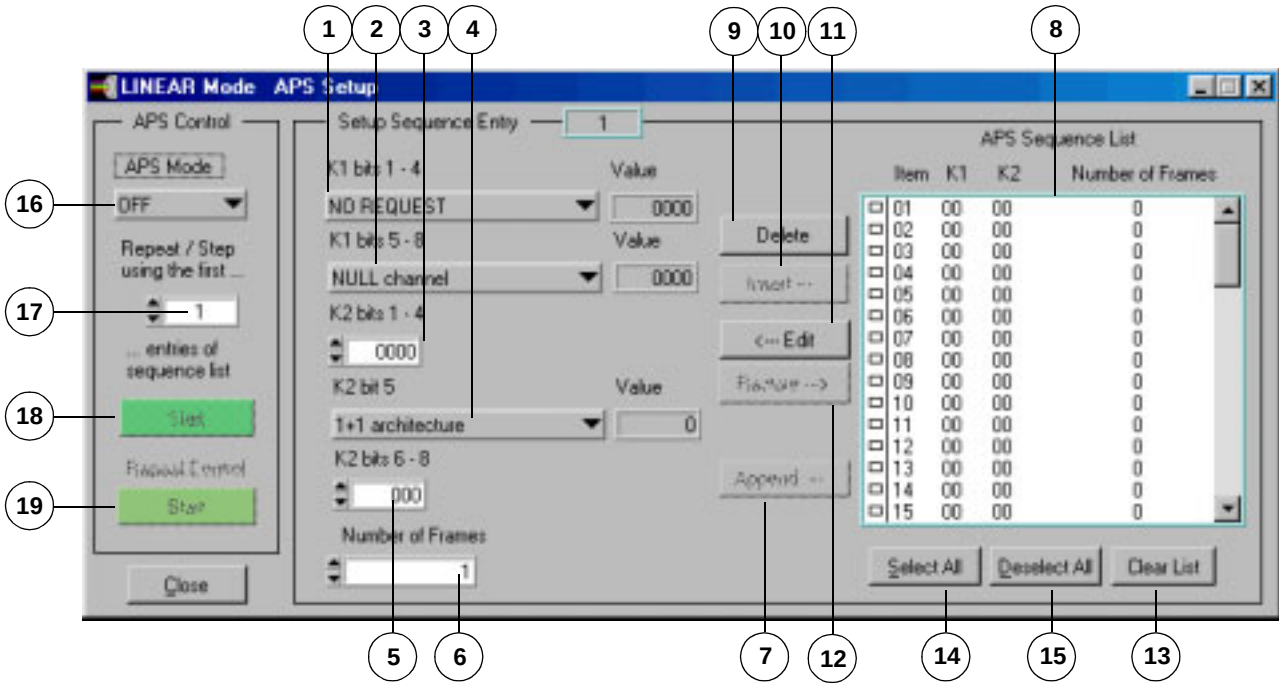


Figure 3-7. APS Setup

1 Select bits 1 to 4 of K1.

2 Select bits 5 to 8 of K1.

3 Select bits 1 to 4 of K2.

4 Select bit 5 of K2.

5 Select bits 6 to 8 of K2.

6 Select the number of frames.

7 Append the sequence set up with steps **(1)** to **(6)** above to the APS sequence list **(8)**.

8 APS sequence list.

9 Delete the highlighted sequence. (To highlight a sequence click on the sequence or the box in the left hand column of the sequence list **(8)**).

10 Insert the sequence set up with steps **(1)** to **(6)** above to the APS sequence list **(8)**. The sequence will be inserted between two highlighted entries. (To highlight a sequence click on the sequence or the box in the left hand column of the sequence list **(8)**).

11 Edit the highlighted sequence. The sequence will be transferred back to the fields **(1)** to **(6)** to be edited. (After the sequence has been edited, click on the Restore key **(12)** to restore the sequence to the list.)

12 Restore the sequence being edited to the list.

13 Clear the sequence list.

14 Select all of the sequence list.

15 Deselect all of the sequence list.

16 Select the APS mode.

17 Set the number (n) of sequences in the list to repeat, where (n) is the first n sequences in the list. (Available only when APS mode **(16)** is set to Repeat.)

18 Start a single sequence (when APS Mode **(16)** is set to Single) or step to the next item (when APS Mode **(16)** is set to Step).

19 Start a repeat sequence (when APS Mode **(16)** is set to Repeat).

User Foreground Payload

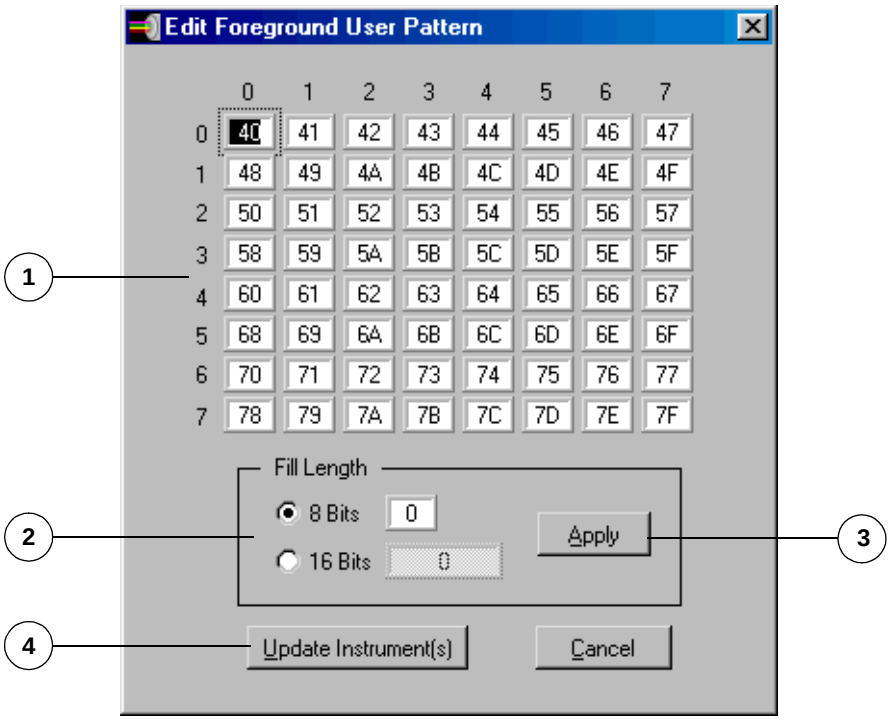


Figure 3-8. Edit Foreground User Pattern

1 User editable bytes.

2 Select 8 or 16 bit fill length.

3 Apply the selected fill length.

4 Update the instrument(s) with the pattern.

User Background Payload

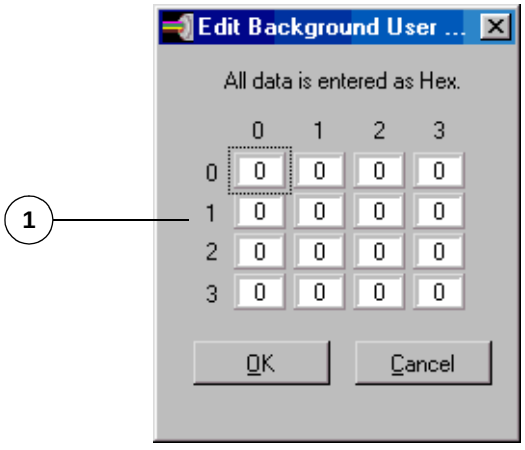


Figure 3-9. Edit Background User Pattern

1 User editable bytes (entered as Hex.)

Receiver Setup

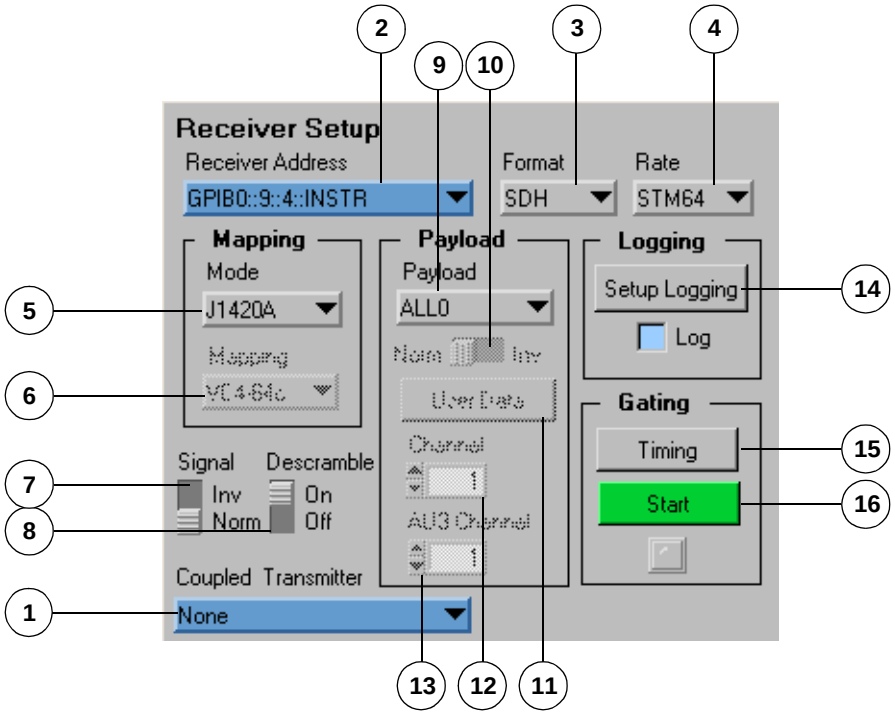


Figure 3-10. Receiver Setup Area

1 Couple this receiver module to a particular transmitter module. (The receiver settings will be set to those of the transmitter.)

2 Select a receiver module.

3 Select the framing format.

4 Select the transmission rate.

5 Select the mapping mode.

6 Select the mapping.

7 Invert the signal.

8 De scramble the frame.

9 Select the payload.

10 Invert the payload.

11 Edit the user pattern when the payload **(9)** is set to User, see Figure 3-11.

12 Select the payload channel. The channel selection range depends on the mapping selected **(5)**.

13 Select the payload AU3 channel when the payload **(6)** is set to VC3.

14 Set up logging, see Figure 3-13.

15 Set up the gating time, see Figure 3-12.

16 Start gating*.

* Where multiple receivers are being used and the GUI is set to control them all, note that gating is not synchronized. If the gating mode is Timed or Single then the receivers will each gate for the correct length of time but the start will not be synchronized. If the gating mode is Manual then it is possible that each receiver will not gate for exactly the same duration.

User Payload Pattern

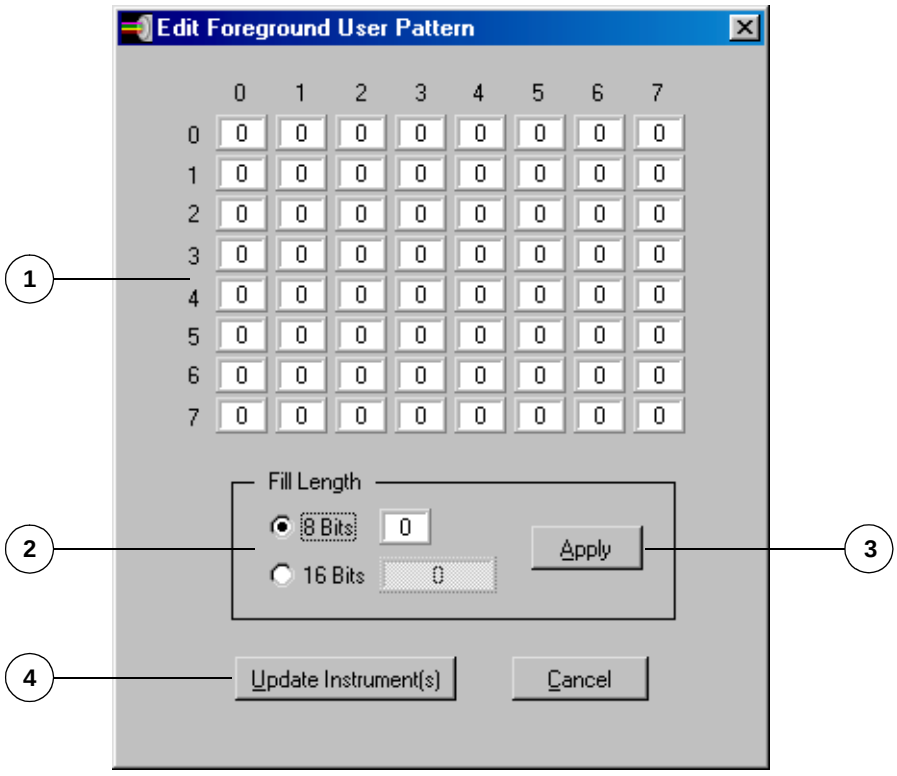


Figure 3-11. Edit Foreground User Pattern

1 User editable bytes.

2 Select 8 or 16 bit fill length.

3 Apply the selected fill length.

4 Update the instrument(s) with the pattern.

Gating Settings

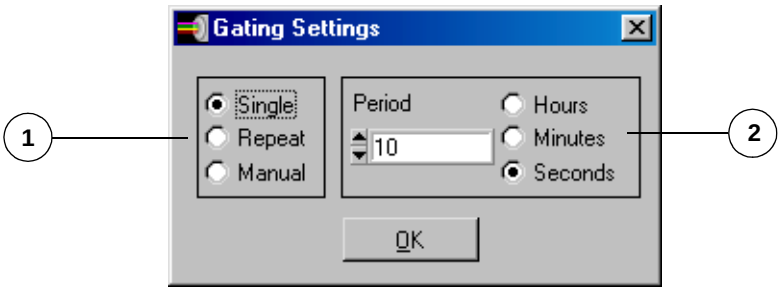


Figure 3-12. Gating Settings

1 Select the gating mode*.

2 Select the gating period.

* Where multiple receivers are being used and the GUI is set to control them all, note that gating is not synchronized. If the gating mode is Timed or Single then the receivers will each gate for the correct length of time but the start will not be synchronized. If the gating mode is Manual then it is possible that each receiver will not gate for exactly the same duration.

Logging Setup

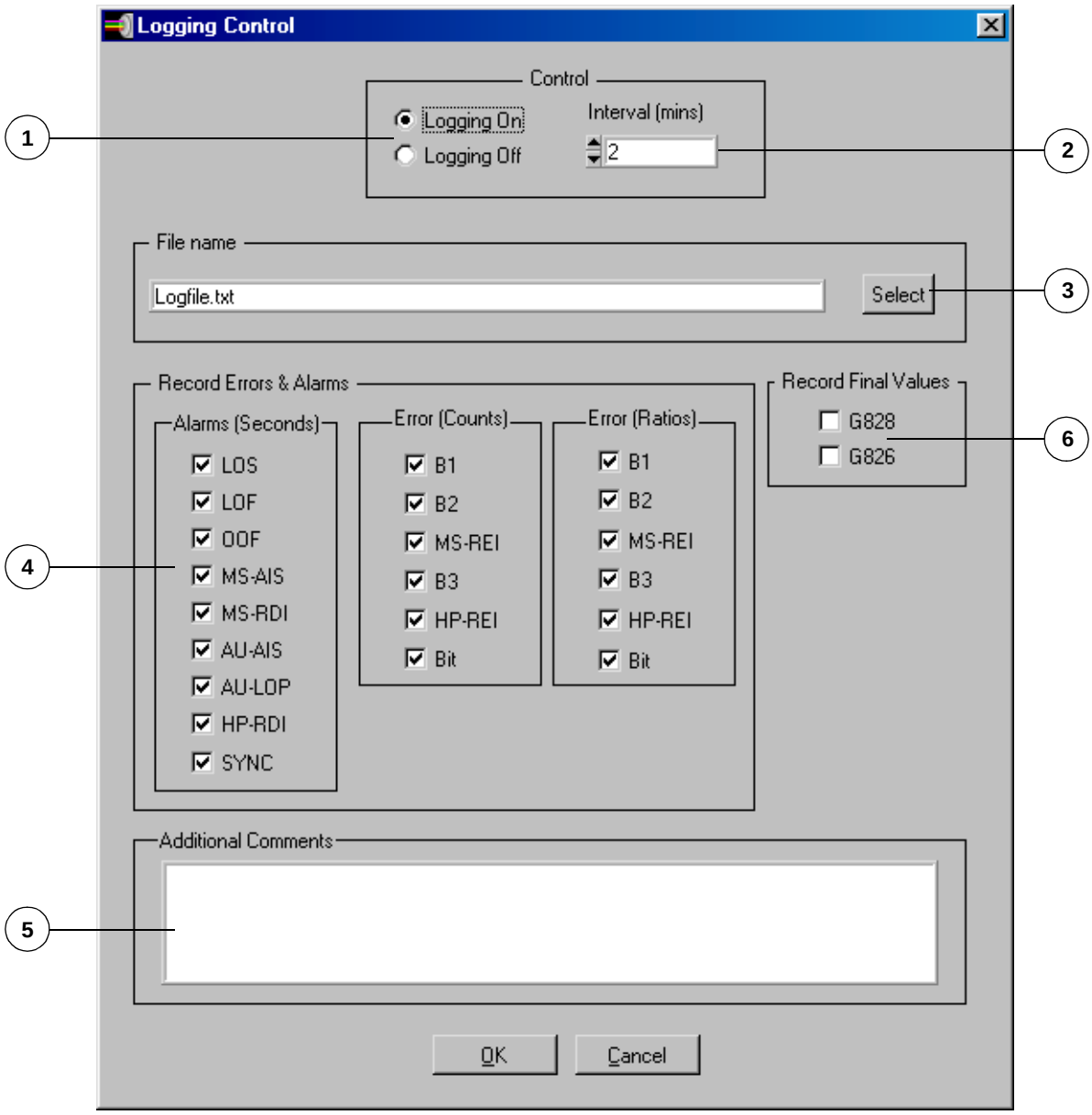


Figure 3-13. Logging Control

1 Set logging on* or off.

2 Set the logging interval† in minutes.

3 Select a file name for the logged data.

4 Select the alarms and errors to log.

5 Type additional comments to be added to the file.

6 Select either G.826 or G.828 final values to be appended to the log file.

* Setting logging on creates two files, a log file and an event file. (The files are identified by “log” or “event” appended to the filename selected in **(3)** above.) The log file summarizes the events occurring in the specified interval and the event file details each event in the specified interval.

† The logging interval is the time period between logging cumulative results to the periodic log file.

Clock Setup

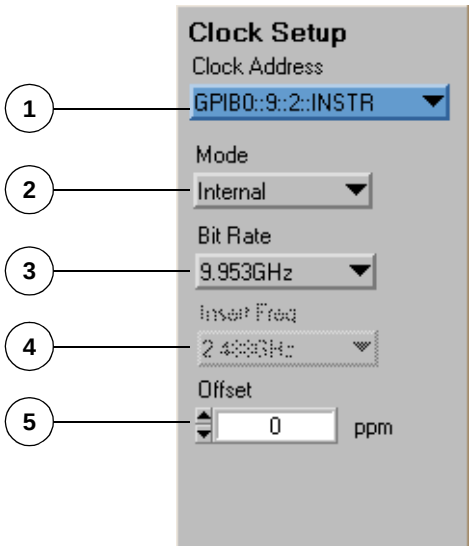


Figure 3-14. Clock Setup Area

1 Select a Clock Source module

2 Select the clock generation Mode (Internal, External, Insert or Slave)

3 Select the Clock Bit Rate.

4 Select the Insert Frequency to the Ref Clock Insert port. (Only enabled when External Insert Mode is selected)

5 Select the frequency Offset

Note When selecting the clock generation Mode **(2)**:

Internal	Refers to the internally generated clock.
External	Refers to the **Clock Ext Clock In** port*.
Insert	Refers to the **Ref Clocks Insert In** port*.
Slave	Refers to the **Ref Clocks Slave In** port*.

* For more detail, refer to the *J1421A/J1422B/J1426A/J1427A 10G SpectralBER Clock Source/MTS/BITS and Transmitter Module User's Manual*

Results

Each page of results contains four separate Results Panels. One Results Panel is highlighted for each Receiver in the system (identified by the GPIB address at the top of the panel). If the system contains more than four Receivers, click on the page Down button at the right hand side of the page to display the next four Receiver Results panels. Figure 3-15 shows the default Errors/Alarms Results Panel. The other results, are obtained by selecting from the **Results Type** pull down menu **(2)** in Figure 3-15. Select from the following:

- Errors/Alarms, see Figure 3-15.
- Service Disruption, see Figure 3-18.
- G826 Analysis, see Figure 3-20.
- G828 Analysis, see Figure 3-21.
- SOH Capture, see Figure 3-24.
- APS, see Figure 3-16.
- J0 Capture, see Figure 3-22.
- Pointers, see Figure 3-19.
- POH, see Figure 3-17.
- J1 Capture, see Figure 3-23.

Errors/ Alarms

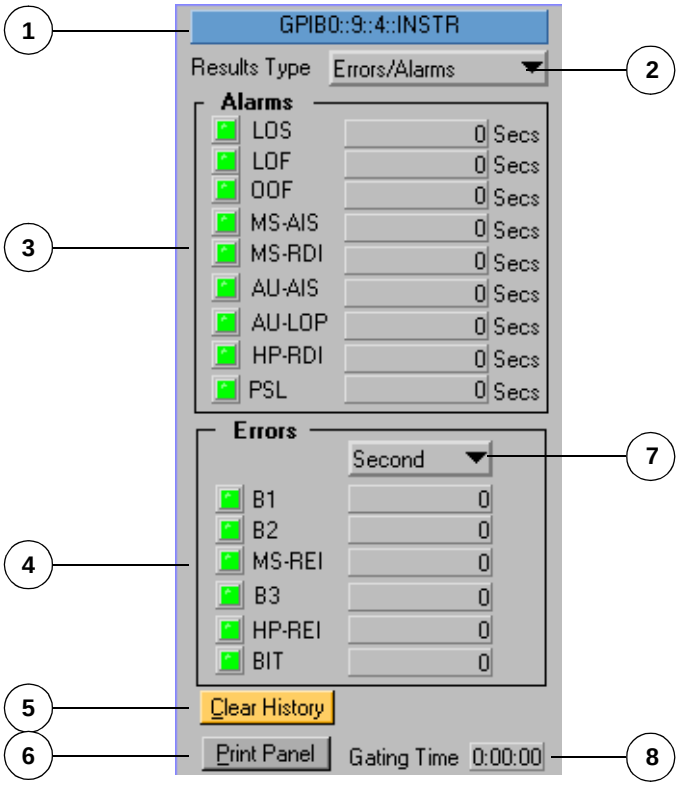


Figure 3-15. Error/Alarm Results

1 Displays the Receiver module address. (The color* of the bar indicates Error/Alarm history.)

2 Select the type of results displayed.

3 Alarm status display*.

4 Error status display*.

5 Clear alarm and error history.

6 Prints this results panel to any connected printer.

7 Select the error measurement mode.

8 Display of elapsed gating time.

* Green indicates no error/alarm, Red indicates an error/alarm and Yellow indicates that there has been an error/alarm during the present gating period. (Starting a new gating period clears existing error and alarm conditions.)

APS

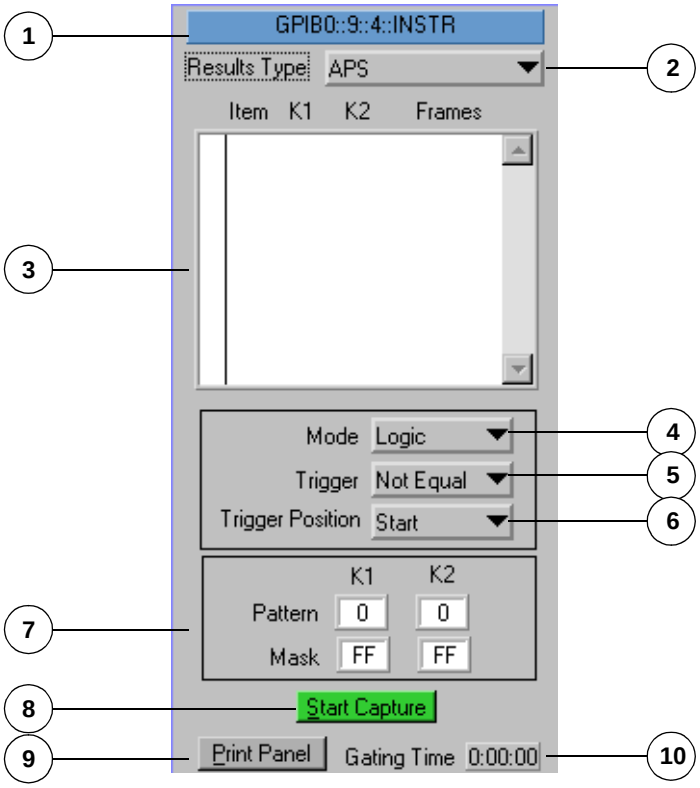


Figure 3-16. APS Results

1 Displays the Receiver module address. (The color* of the bar indicates Error/Alarm history.).

2 Select the type of results displayed.

3 Display of APS sequence.

4 Select mode.

5 Select trigger.

6 Select trigger position.

7 Edit the K1 and K2 pattern and mask.

8 Start/Stop APS capture.

9 Prints this results panel to any connected printer.

10 Display of elapsed gating time.

* Green indicates no error/alarm, Red indicates an error/alarm and Yellow indicates that there has been an error/alarm during the present gating period. (Starting a new gating period clears existing error and alarm conditions.)

POH

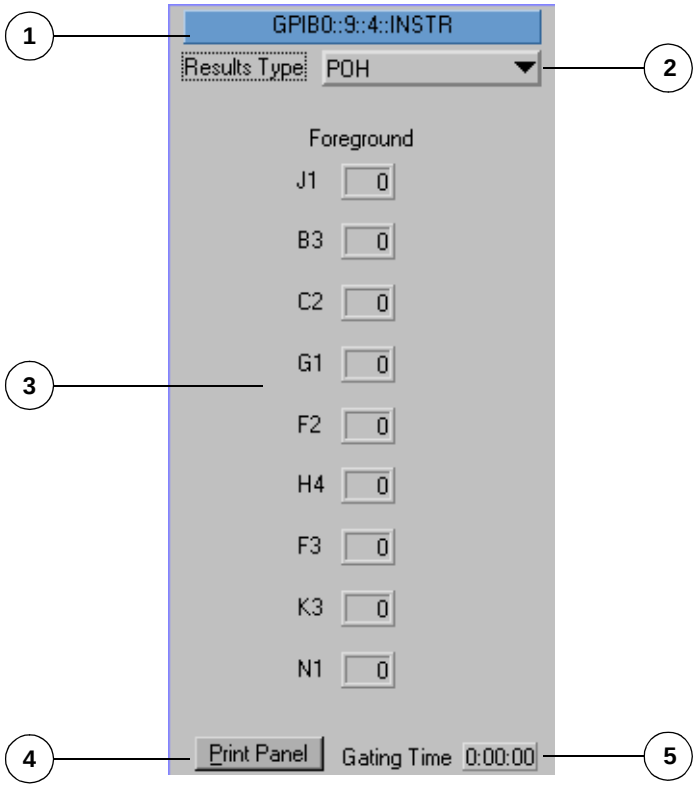


Figure 3-17. POH Results

1 Displays the Receiver module address. (The color* of the bar indicates Error/Alarm history.)

2 Select the type of results displayed.

3 Display of POH bytes.

4 Prints this results panel to any connected printer.

5 Display of elapsed gating time.

* Green indicates no error/alarm, Red indicates an error/alarm and Yellow indicates that there has been an error/alarm during the present gating period. (Starting a new gating period clears existing error and alarm conditions.)

Service Disruption

The service disruption measurement uses payload bit errors to determine the impact on a service caused by a network fault, for example, a fiber break and it's subsequent restoration (a protection switch).

- The service disruption begins and ends with a payload bit error. Error bursts of less than 10 µs are ignored.
- Error bursts are assumed to have completed when >200 ms elapse without any payload bit errors being received.
- The longest burst detected is 2 seconds with 1 micro second resolution.
- Measurement accuracy is ±0.01% of reading ±30 µs.

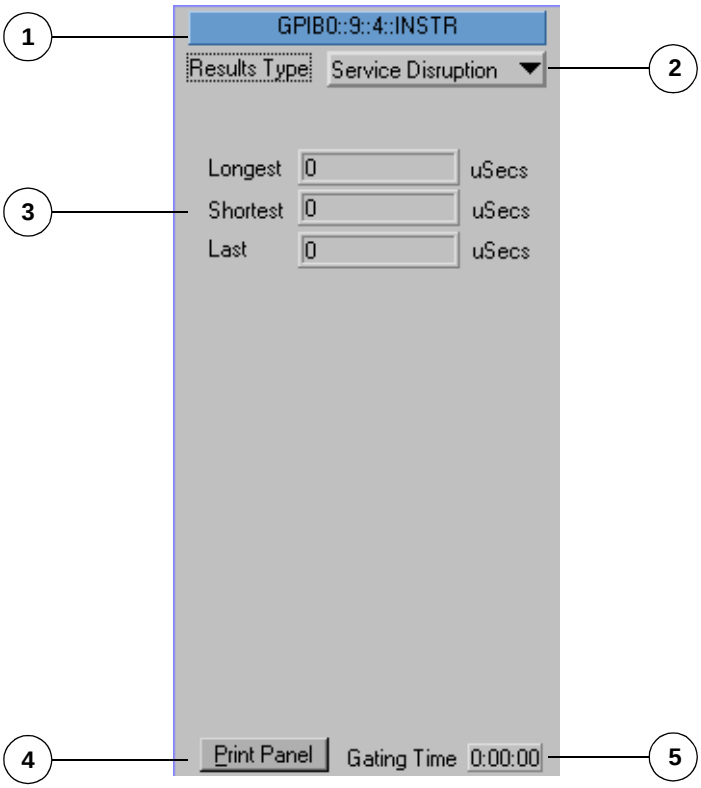


Figure 3-18. Service Disruption Results

1 Displays the Receiver module address. (The color* of the bar indicates Error/Alarm history.)

2 Select the type of results displayed.

3 Display of Service Disruption results.

4 Prints this results panel to any connected printer.

5 Display of elapsed gating time.

* Green indicates no error/alarm, Red indicates an error/alarm and Yellow indicates that there has been an error/alarm during the present gating period. (Starting a new gating period clears existing error and alarm conditions.)

Pointers

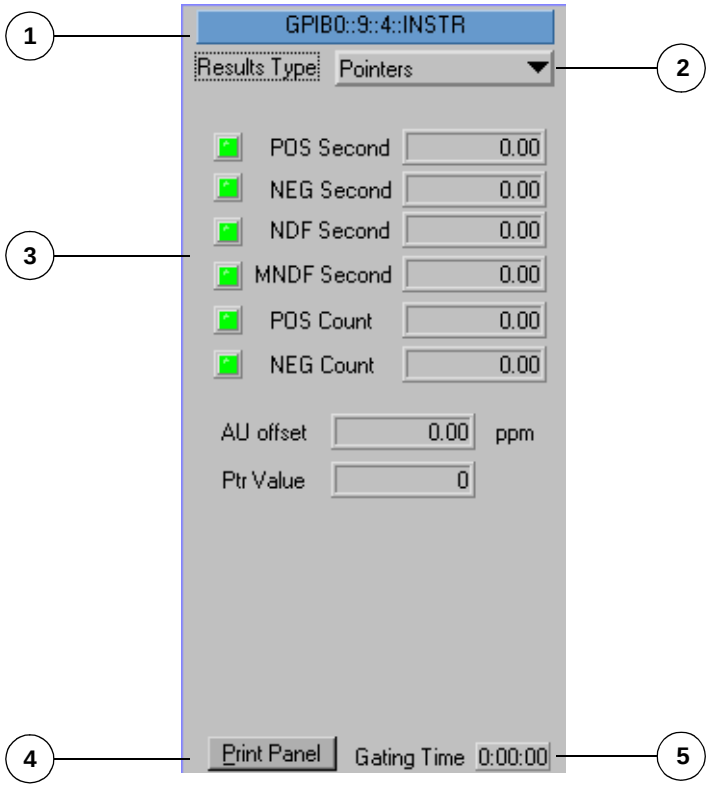


Figure 3-19. Pointers Results

1. Displays the Receiver module address. (The color* of the bar indicates Error/Alarm history.)
2. Select the type of results displayed.
3. Display of Pointers results*.
4. Prints this results panel to any connected printer.
5. Display of elapsed gating time.

* Green indicates no event, Red indicates an event and Yellow indicates that there has been an event during the present gating period. (Starting a new gating period clears existing status conditions.)

G826 Analysis

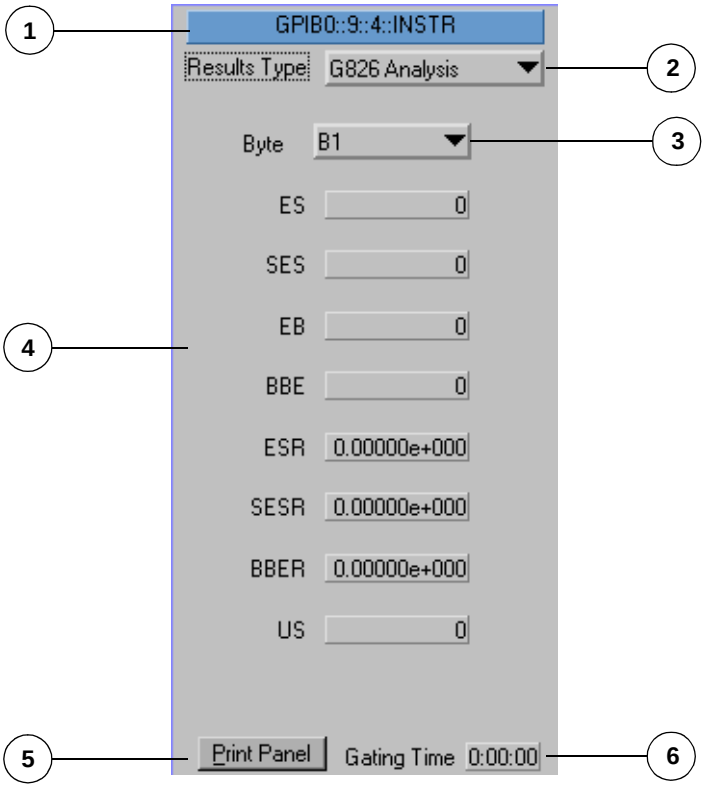


Figure 3-20. G826 Analysis Results

1 Displays the Receiver module address. (The color* of the bar indicates Error/Alarm history.)

2 Select the type of results displayed.

3 Select which byte to look at (B1, B2, B3, MS-REI, HP-REI)

4 Display of G826 Analysis results.

5 Prints this results panel to any connected printer.

6 Display of elapsed gating time.

* Green indicates no error/alarm, Red indicates an error/alarm and Yellow indicates that there has been an error/alarm during the present gating period. (Starting a new gating period clears existing error and alarm conditions.)

G828 Analysis

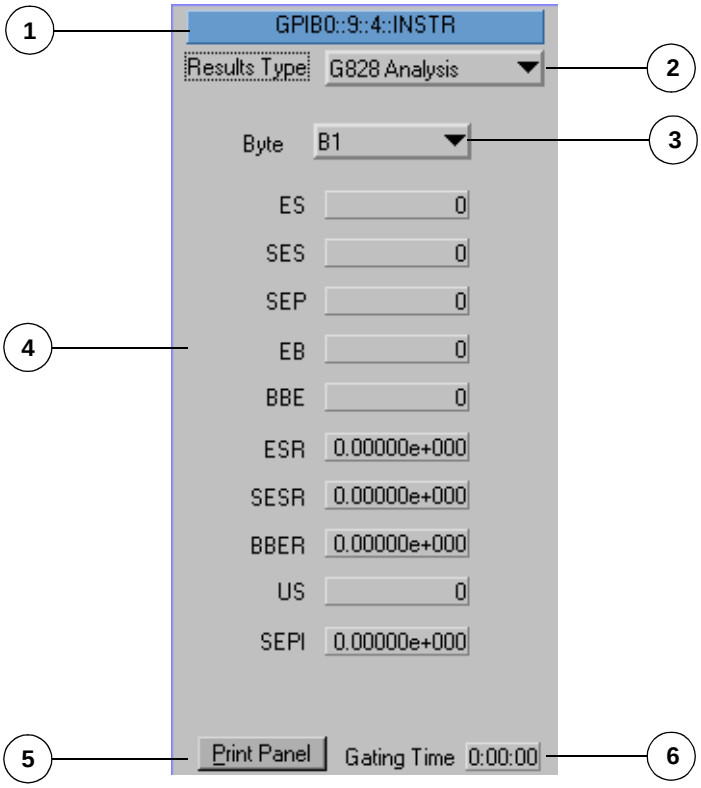


Figure 3-21. G828 Analysis Results

1 Displays the Receiver module address. (The color* of the bar indicates Error/Alarm history.)

2 Select the type of results displayed.

3 Select which byte to look at (B1, B2, B3, MS-REI, HP-REI)

4 Display of G828 Analysis results.

5 Prints this results panel to any connected printer.

6 Display of elapsed gating time.

* Green indicates no error/alarm, Red indicates an error/alarm and Yellow indicates that there has been an error/alarm during the present gating period. (Starting a new gating period clears existing error and alarm conditions.)

J0 Capture

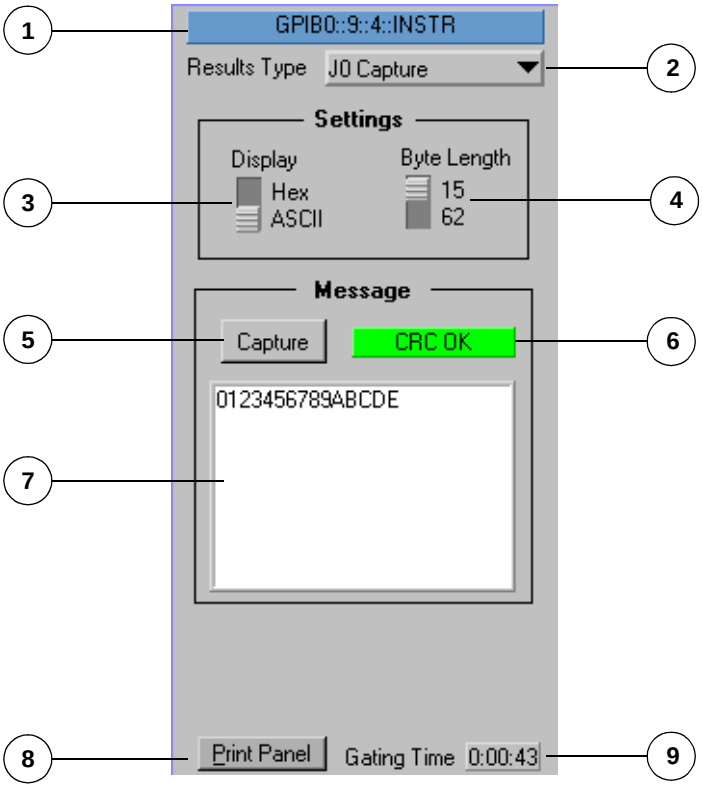


Figure 3-22. J0 Capture Results

1. Displays the Receiver module address. (The color* of the bar indicates Error/Alarm history.)
2. Select the type of results displayed.
3. Set the Display string format to ASCII or Hex.
4. Set the Byte length of the data string to 15 or 62† when in ASCII mode or to 16 or 64* when in Hex mode.
5. Capture the transmitted J0 string.
6. Display of either CRC† or CR+LF† status‡.
7. Display of J0 string.
8. Prints this results panel to any connected printer.
9. Display of elapsed gating time.

---

* Green indicates no error/alarm, Red indicates an error/alarm and Yellow indicates that there has been an error/alarm during the present gating period. (Starting a new gating period clears existing error and alarm conditions.)

† In the transmitter, when the string format is set to ASCII and the data length to 15, CRC is calculated and added to the transmitted string. When the string format is set to ASCII and the data length to 62, CR+LF is added to the transmitted string. When the string format is set to Hex and the data length to either 16 or 64, the string is sent as specified with no addition.

‡ Green indicates no error and Red indicates an error.

J1 Capture

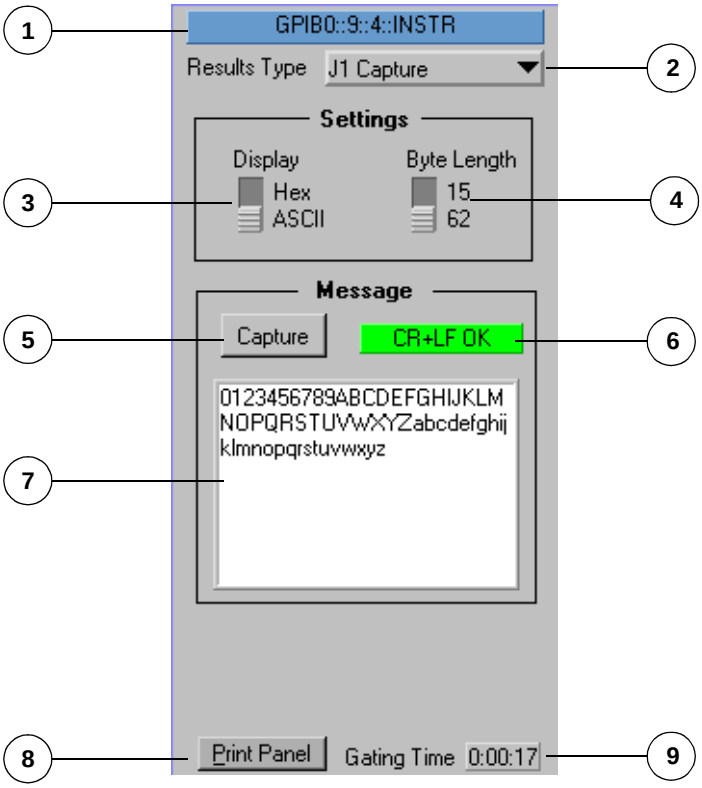


Figure 3-23. J1 Capture Results

1. Displays the Receiver module address. (The color* of the bar indicates Error/Alarm history.)
2. Select the type of results displayed.
3. Set the Display string format to ASCII or Hex.
4. Set the Byte length of the data string to 15 or 62† when in ASCII mode or to 16 or 64* when in Hex mode.
5. Capture the transmitted J1 string.
6. Display of either CRC† or CR+LF† status‡.
7. Display of J1 string.
8. Prints this results panel to any connected printer.
9. Display of elapsed gating time.

---

* Green indicates no error/alarm, Red indicates an error/alarm and Yellow indicates that there has been an error/alarm during the present gating period. (Starting a new gating period clears existing error and alarm conditions.)

† In the transmitter, when the string format is set to ASCII and the data length to 15, CRC is calculated and added to the transmitted string. When the string format is set to ASCII and the data length to 62, CR+LF is added to the transmitted string. When the string format is set to Hex and the data length to either 16 or 64, the string is sent as specified with no addition.

‡ Green indicates no error and Red indicates an error.

SOH Capture

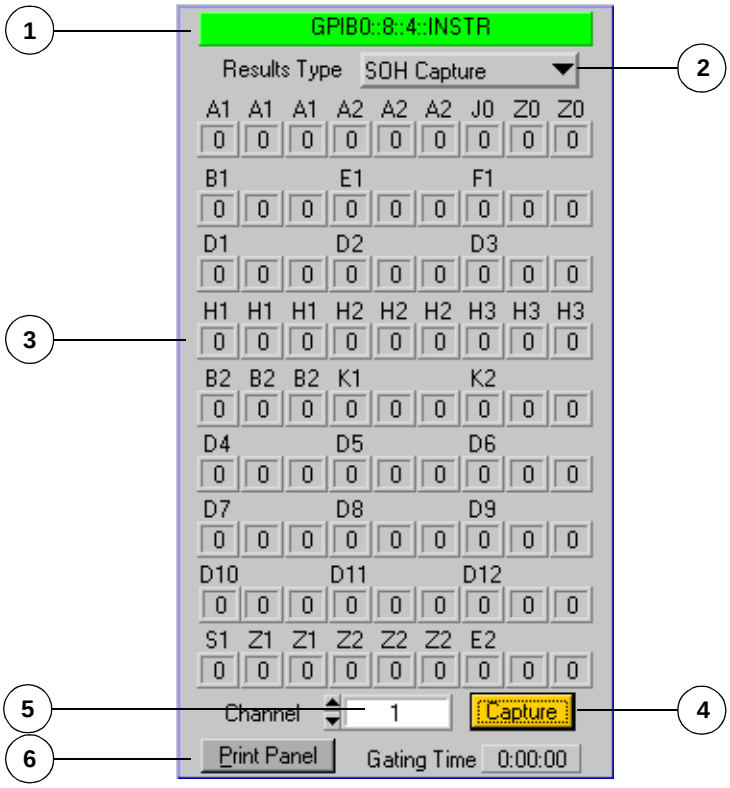


Figure 3-24. SOH Capture Results

1 Displays the Receiver module address. (The color* of the bar indicates Error/Alarm history.)

2 Select the type of results displayed.

3 Display of SOH Capture.

4 Capture SOH Results.

5 Enter the STS-3/STM-1 channel number.

6 Prints this results panel to any connected printer.

* Green indicates no error/alarm, Red indicates an error/alarm and Yellow indicates that there has been an error/alarm during the present gating period. (Starting a new gating period clears existing error and alarm conditions.)

Chapter 4
Using the Universal Instrument Driver

Introduction

The Agilent SpectralBER system can be controlled from a PC or workstation using either SCPI commands, Universal Instrument Drivers or manually using a graphical user interface (soft front panel). This chapter describes using the Universal Instrument Driver.

For more information on using SCPI commands, see Chapter 5 "Example Programs using SCPI" on page 57 and the *SpectralBER System (10 Gb/s) Remote Control Manual*. For more information on the Graphical User Interface, see Chapter 3 "The Soft Front Panel (GUI)" on page 55.

The Universal Instrument Driver (UID) HPJ142xb complies with the following:

- VXIplug&play WIN 95 and WIN NT System Frameworks.
- VISA revision 1.0.
- HPJ142xb Firmware.

The following information is common to all programs that use the HPJ142xb instrument driver. More detailed information will be found in the on-line help file that complements this manual. The on-line help file (HPJ142xb.hlp) presents more application programming examples, a cross-reference between instrument commands and driver functions, and detailed documentation of each function.

Note Under Solaris, view the *HPJ142xa(b).hlp* file with the command: *hyperlink* or *hyperhelp HPJ142xa(b).hlp* or *vi HPJ142xa(b).txt.*

VISA, VXIplug&play and the UID

The HPJ142xb Universal Instrument Driver (UID) conforms to the VXIplug&play driver standard except that there is no VXIplug&play compatible soft front panel and no knowledge base file.

1. It is built on top of, and uses the services provided by VISA. VISA supports GPIB and VXI protocols. The driver can be used with any GPIB card for which the manufacturer has provided a VISA DLL.

2. It includes a "Function Panel" (.fp) file which allows it to be used with visual programming environments such as HP-VEE, LabWindows, and LabVIEW.

3. It includes a comprehensive on-line help file to complement this manual. The help file presents application programming examples, a cross-reference between instrument commands and drive functions, and detailed documentation of each function.

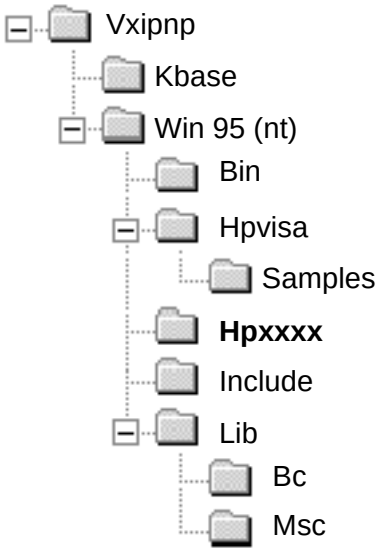
4. The source code is included so that the driver can be modified if desired. The source conforms to VXIplug&play standards. Modifications should only be made by people who are familiar with the VXIplug&play standard.

5. It includes a Visual Basic include file (.bas) which contains the function calls in Visual Basic syntax, so that driver functions can be called from Visual Basic. If you use Visual Basic with this driver, you should be familiar with C/C++ function declarations. In particular, care must be taken when working with C/C++ pointers.

Directory Structure

Windows

The setup program which installs the HPJ142xb instrument driver creates the standard directory structure for VXIplug&play drivers if it does not already exist. The structure for the Windows 95 and Windows NT Vxipnp subdirectory tree is:



Windows Directory Structure

In the directory example above, Hpxxxx is a place holder for the actual directory named HPJ142xb containing the instrument driver. There is a directory for each instrument driver.

Solaris

The VXI*plug&play* specification requires that the environment variable *VXIPNPPATH* be defined in the */etc/profile* file. For HP-UX 10.01 and above the required value is */opt/vxipnp*.

The base directory for each instrument is:

$VXIPNPPATH/hpux/<inst_name>

All shared library files with the *.sl* extension go in:

$VXIPNPPATH/hpux/bin

All *.h* files go in:

$VXIPNPPATH/hpux/include

All other HP VISA files go in:

$VXIPNPPATH/hpux/hpvisa

Opening an Instrument Session

Introduction

To control an instrument from a program, a communication path between the computer/controller and the instrument must be opened. This path is known as an instrument session and is opened with the function:

```
ViStatus hpj422xa_init( ViRsrc InstrDesc, ViBoolean id_query, ViBoolean reset, ViPSession vi );
```

or

```
ViStatus HPJ142xb_init( ViRsrc InstrDesc, ViBoolean id_query, ViBoolean reset, ViPSession vi );
```

Instruments are assigned a handle when the instrument session is opened. The handle is used to identify this particular instrument in all subsequent calls to driver functions.

The parameters of function hpj422xa_init/HPJ142xb_init include:

ViRsrc InstrDesc the address of the instrument.

ViBoolean id_query a Boolean flag which indicates if in-system verification should be performed. Passing VI_TRUE (1) will perform an in-system verification. Passing VI_FALSE (0) will not. If you set id_query to false it is possible to use the generic functions of the instrument driver with other instruments.

ViBoolean reset a Boolean flag which indicates if the instrument should be reset when it is opened. Passing VI_TRUE (1) will perform a reset when the session is opened. Passing VI_FALSE (0) will not perform a reset.

ViPSession vi a pointer to an instrument session. vi is the handle which addresses the instrument and is the first parameter passed in all driver functions.

Successful completion of this function returns VI_SUCCESS.

For more information see “Examples” on page 53.

Examples

The address strings for the various interfaces are given below. In each string, 'INSTR' is a VISA resource type. If you want to be compatible with future releases of VISA you must include the INSTR parameter in the syntax.

Note In the following examples **hpjnnnxa** is a place holder for and can be substituted with **HPJ142xb**.

GPIB Addressing

Used when programming instruments using a GPIB interface:

GPIB[board]::logical address[::secondary address][::INSTR]

Visual C++ Programming Example

```
/* example uses default GPIB board number for a single interface board */
ViSession vi;
ViStatus vistat;
if ((vistat = hpjnnnxa_init("GPIB0::AA::INSTR", 0, 0, &vi)) != VI_SUCCESS)
{
 /* handle error here, vistat contains return error code */
}
```

Visual BASIC Programming Example

```
Dim vi As Long
Dim errStatus As Long
errStatus = hpjnnnxa_init("GPIB0::AA::INSTR", 0, 0, vi)
```

Closing an Instrument Session

Sessions (vi) opened with the hpjnnnxa_init() function are closed with the function:

hpjnnnxa_close(ViSession vi);

When no further communication with an instrument is required, the session must be explicitly closed (hpjnnnxa_close() function). VISA does not remove sessions unless they are explicitly closed. Closing the instrument session frees all data structures and system resources allocated to that session.

Error Handling

Events and errors within a instrument control program can be detected by polling the instrument. The example programs poll (query) the instrument after each function to determine if an error or other event has occurred. Polling is used in application development environments (ADEs) that do not support asynchronous activities where callbacks can be used. The example programs set up and use polling as shown below.

1. Declare a variable to contain the function completion code.

```
ViStatus errStatus;
```

Every driver function returns the completion code ViStatus. If the function executes with no I/O errors, driver errors, or instrument errors, ViStatus is 0 (VI_SUCCESS). If an error occurs, ViStatus is a negative error code. Warnings are positive error codes, and indicate the operation succeeded but special conditions exist.

2. Enable automatic instrument error checking following each function call.

```
hpjnnnxa_errorQueryDetect(vi, VI_TRUE);
```

When enabled, the driver queries the instrument for an error condition before returning from the function. If an error occurred, errStatus (Step 1) will contain a code indicating that an error was detected (hpjnnnxa_INSTR_ERROR_DETECTED).

3. Check for an error (or event) after each function.

```
errStatus = hpjnnnxa_cmd(vi, "MEAS:FREQ");
check(vi, errStatus);
```

After the function executes, errStatus contains the completion code. The completion code and instrument id are passed to an error checking routine. In the above statement, the routine is called 'check'.

4. Create a routine to respond to the error or event. The following routine is used to read errors.

Example

```
void check (ViSession vi, ViStatus errStatus)
{
 /* variables for error code and message */
 ViInt32 inst_err;
 ViChar err_message[256];

 /* VI_SUCCESS is 0 and is defined in VISATYPE.h */
 if(VI_SUCCESS > errStatus)
 {
   /* send a device clear - to ensure communication with the instrument */
   hpjnnnxa_dcl(vi);

   /* hpjnnnxa_INSTR_ERROR_DETECTED defined in hpjnnnxa.h */
   if(hpjnnnxa_INSTR_ERROR_DETECTED == errStatus)
   {
    /* query the instrument for the error */
    hpjnnnxa_error_query(vi, &inst_err, err_message);

    /* display the error */
    printf("Instrument Error : %ld, %s\n", inst_err, err_message);
   }
   else/* driver error */
   {
    /* get the driver error message */
    hpjnnnxa_error_message(vi, errStatus, err_message);

    /* display the error */
    printf("Driver Error : %ld, %s\n", errStatus, err_message);
   }
   /* optionally reset the instrument, close the instrument handle */
   hpjnnnxa_reset(vi);
   hpjnnnxa_close(vi);
   exit(1);
 }
 return;
}
```

Chapter 5
Example Programs using SCPI

Introduction

The Agilent SpectralBER system can be controlled from a PC or workstation using either SCPI commands, Universal Instrument Drivers or manually using a Graphical User Interface (or soft front panel). This chapter provides examples of how SCPI commands can be used to control the system.

For more information on using SCPI commands, see Example Programs using SCPI page 57 and either the *SpectralBER System (2.5 Gb/s and below)* or *SpectralBER System (10 Gb/s) Remote Control Manual*. For more information on the Graphical User Interface, see The Soft Front Panel (GUI) page 55. For more information on the Universal Instrument Drivers, see Using the Universal Instrument Driver page 49.

The examples given here are written in “C”, but the general principles and sequence of SCPI commands apply to and can be adapted easily to other programming languages.

Start Gating

This program illustrates the sequence of SCPI commands required to start a 10 Gb/s System gating.

```
/*"start_gating.c"
  This example program starts the SpectralBER system gating.
                    Note: You must change the address to suit your system.) */

#include <conio.h>
#include <stdio.h>
#include "c:\vxipnp\win95\include\visa.h"    /* Change the file path to suit.
                           Note: This header file is supplied with HP Visa. */

void main () {

  ViSession defaultRM, vi;

  /* Open session to GPIB device (Change the address to suit)*/
  viOpenDefaultRM (&defaultRM);
  viOpen (defaultRM, "GPIB0::09::01::INSTR", VI_NULL,VI_NULL, &vi);

  /* Initialize device */
  viPrintf (vi, "*RST\n");

  /* Set Maximum Measurement Period */
  viPrintf (vi, ":SOUR5:PULS2:PER 3596400\n");

  /* Disable 100ms Heartbeat generation */
  viPrintf (vi, ":OUTP5:TTLT0 OFF\n");

  /* Disable Synchronous Pulse generation */
  viPrintf (vi, ":OUTP5:TTLT1 OFF\n");

  /* Disable 100ms Heartbeat control system */
  viPrintf (vi, ":INIT2:CONT OFF\n");

  /* Disable Synchronous Command Pulse system */
  viPrintf (vi, ":INIT3:CONT OFF\n");

  /* Set Idle state for Trigger 2 system */
  viPrintf (vi, ":ABOR2\n");

  /* Set Idle state for Trigger 3 system */
  viPrintf (vi, ":ABOR3\n");

  /* Select source of Trigger 2 system */
  viPrintf (vi, ":TRIG2:SOUR TTL0\n");

  /* Enable 100ms Heartbeat control system */
  viPrintf (vi, ":INIT2:CONT ON\n");

  /* Enable Synchronous Command Pulse system */
  viPrintf (vi, ":INIT3:CONT ON\n");
```

```
  /* Enable 100ms Heartbeat generation */
  viPrintf (vi, “:OUTP5:TTLT0 ON\n”);

  /* Enable Synchronous Pulse generation */
  viPrintf (vi, “:OUTP5:TTLT1 ON\n");

  /* Set Synchronous Command to start */
  viPrintf (vi, “:TRIG3:COMM START\n”);

  /* Issue a Synchronous Pulse to START */
  viPrintf (vi, “:OUTP5:TTLT1:IMM\n”);

  /* Close session */
  viClose (vi);
  viClose (defaultRM);
}
```

Stop Gating

This program illustrates the sequence of SCPI commands required to stop a 10 Gb/s System gating.

```
/*"stop_gating.c"
  This example program stops the SpectralBER system gating.
                    Note: You must change the address to suit your system.) */

#include <conio.h>
#include <stdio.h>
#include "c:\vxipnp\win95\include\visa.h"     /* Change the file path to suit */
                           Note: This header file is supplied with HP Visa. */

void main () {

  ViSession defaultRM, vi;

 /* Open session to GPIB device (Change the address to suit)*/
  viOpenDefaultRM (&defaultRM);
  viOpen (defaultRM, "GPIB0::09::01::INSTR", VI_NULL,VI_NULL, &vi);

  /* Set Synchronous Command to STOP */
  viPrintf (vi, ":TRIG3:COMM STOP\n");

  /* Issue a Synchronous Pulse to STOP */
  viPrintf (vi, ":OUTP5:TTLT1:IMM\n");

  /* Issue a Synchronous Pulse to STOP */
  viPrintf (vi, ":OUTP5:TTLT1 OFF\n");

  /* Disable 100ms Heartbeat control system */
  viPrintf (vi, ":INIT2:CONT OFF\n");

  /* Disable Synchronous Command Pulse system */
  viPrintf (vi, ":INIT3:CONT OFF\n");

  /* Ensure Heartbeat system is IDLE */
  viPrintf (vi, ":ABORT2\n");

  /* Ensure Synchronous Command System is IDLE*/
  viPrintf (vi, ":ABORT3\n");

  /* Close session */
  viClose (vi);
  viClose (defaultRM);
}
```

Chapter 6
Firmware Upgrade Utility

The Firmware Upgrade Utility is provided so that you can easily upgrade your Agilent SpectralBER module firmware.

Running the Firmware Upgrade Utility

1. Locate the executable file *upgradeutility.exe* in the directory Hpj142xb and start the utility to display the window shown in Figure 6-1.

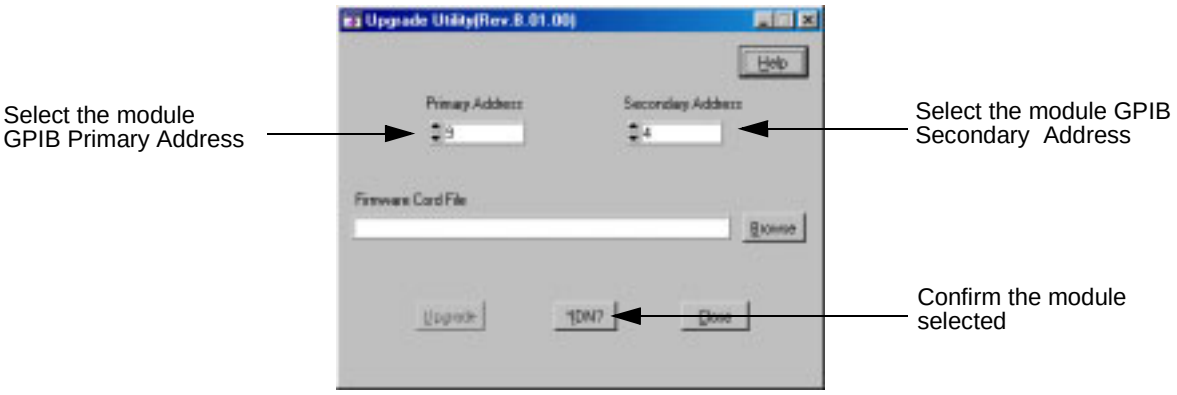


Figure 6-1. Upgrade Utility

2. Select the primary and secondary GPIB addresses of the module to be upgraded and click on the ***IDN?** button to confirm the module as shown in Figure 6-2.

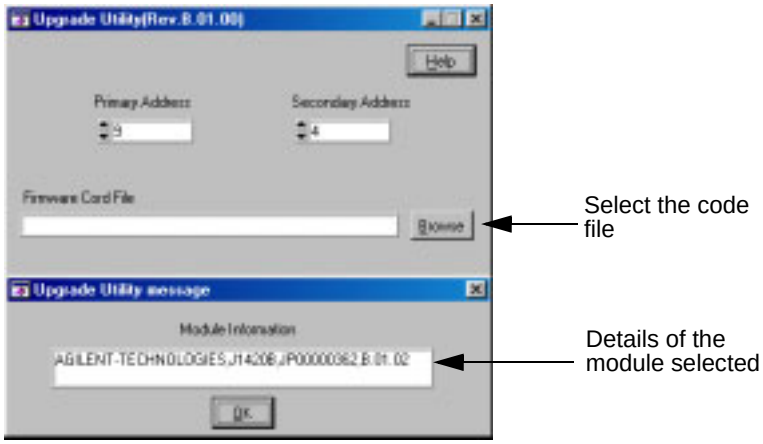


Figure 6-2. Select the Module

3. Select the Firmware Code File by using the **Browse** button to display the File Selection window shown in Figure 6-3.

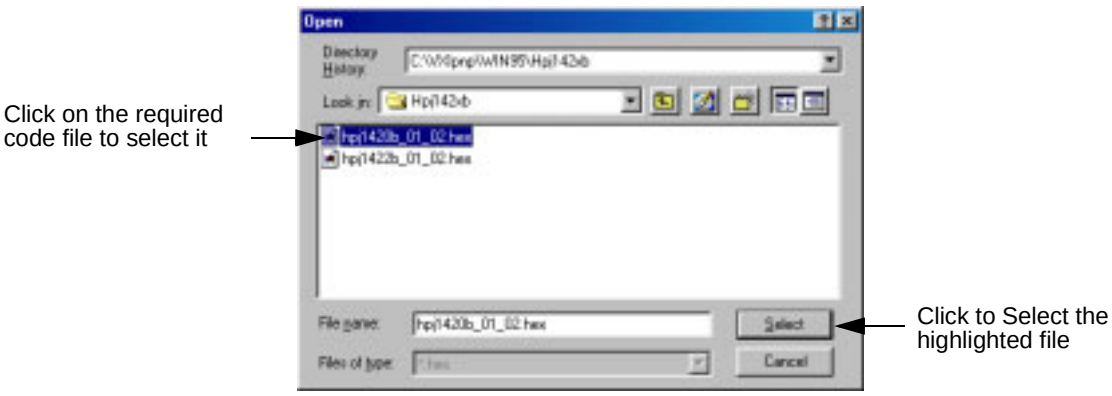


Figure 6-3. Firmware Code File Selection

4. Click on the required code file, then click the **Select** button which will produce the "Upgrade Utility" window as shown in Figure 6-4.

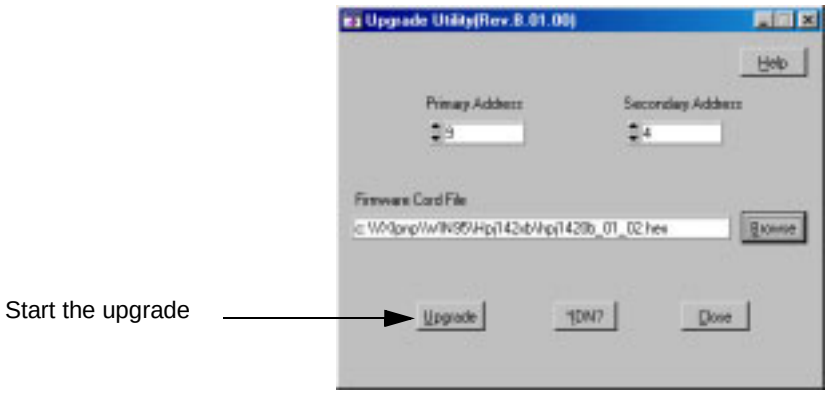


Figure 6-4. Start the Upgrade

5. Click on the **Upgrade** button to start the firmware upgrade process. A message "Erasing flash memory …" will be displayed, followed by a message displaying the progress of the upgrade.

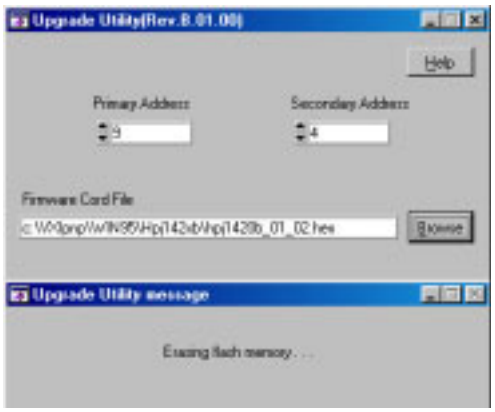


Figure 6-5. Erasing flash memory

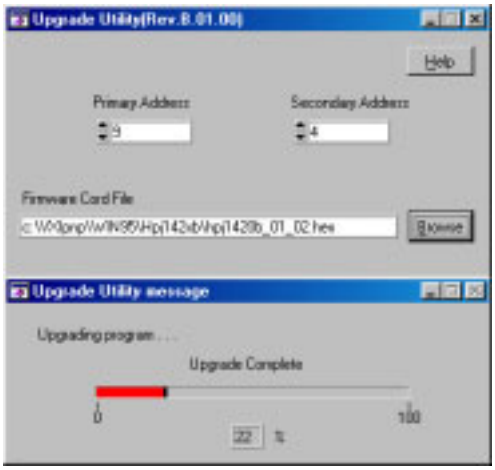


Figure 6-6. Upgrade Progress

The upgrade will take some time to complete, depending on the specification of your external controller, then the final window indicating successful completion of the firmware upgrade will be displayed. If necessary repeat the above process for other modules in the system.

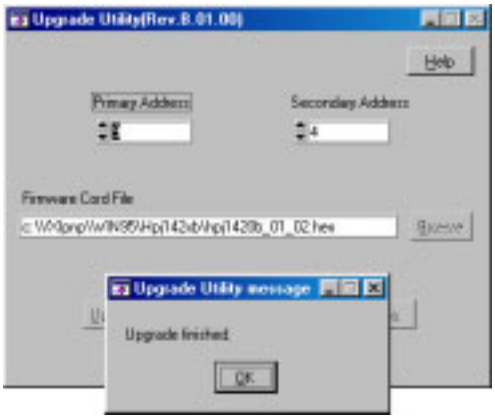


Figure 6-7. Upgrade finished

Index

S

T

U

V

W